

CGS-808

Intelligent Color Graphics

Hardware Manual

Biotech Electronics

CGS-808
HARDWARE MANUAL

Biotech Electronics
P.O. Box 485
Ben Lomond, California 95005
(408) 338-2686
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1.0 INTRODUCTION AND GENERAL INFORMATION

1.1 Introduction

This manual was created for CGS-808 owners and contains all the necessary information to assemble, test, trouble-shoot and modify your color graphics board. In order to obtain the best picture possible and isolate any potential faults, test/diagnostic programs have been included in the software manual to be used after assembly. Be sure to read the entire manual before beginning assembly.

1.2 General Information

1.2.1 CGS-808 General Description

The CGS-808 is a powerful, integrated, intelligent color graphics board for the S-100 bus. It will operate in any S-100 microcomputer or as a stand-alone video processor. It contains its own on-board microprocessor, requires no memory space, and eliminates the need for software driver routines. By changing the firmware pack, the CGS-808 can be upgraded to perform complex graphic functions or custom video processing.

The CGS-808 generates an 8 color display with 12 different programmable and software selectable modes.

The CGS-808 is designed for a high quality, professional display for applications in medicine, business, education, science, industry, and video games.

1.2.2 Receiving Information

Biotech Electronics insures all product leaving its door. As soon as you receive your CGS-808, inspect the package and its contents for damage during shipment. If damage has occurred, contact the factory immediately and the necessary steps will be taken.

1.2.3 Warranty Information

In bare "kit" purchases, the printed circuit board is warranted for 60 days following the date of purchase. Due to the static sensitive nature of MOS chips, the IC's supplied with the bare "kit" are not warranted. All units assembled and tested by Biotech Electronics are warranted for 90 days following the date of purchase. Refer to Appendix J for detailed warranty information.

1.2.4 Factory Service

Factory repair service is provided for out-of-warranty product upon request. Call the factory for a cost estimate and return authorization number, then ship prepaid to Biotech Electronics. Be sure to provide static protection for the board during shipment. Upon repair, the product will be shipped back prepaid.

CGS-808 TECHNICAL SPECIFICATIONS

Following are the technical specifications of the
CGS-808:

- Bus: S-100 (Meets IEEE bus standard).
- I/O Port: 2 I/O ports. Switch selected I/O address boundaries can be located anywhere in I/O address space. One 8 bit parallel I/O expansion port.
- On-Board Processor: 8085 CPU (3MHz).
- Processor RAM: 1,024 bytes static RAM (2114's).
- Processor ROM: Firmware Pack I - 1,024 bytes ROM, Firmware Pack II - 2,048 bytes ROM. Up to 4,096 bytes of ROM.
- Screen Refresh RAM: 6,144 bytes static RAM (2114's).
- Color Graphics Chip: Motorola MC6847.
- Colors Available: Green, yellow, blue, red, buff, cyan, magenta, orange.
- Video Output: Composite 75 ohm video (NTSC Standard). Separated R-Y, B-Y and Y output requires RBY Adapter for connection to a monitor.
- Alphanumerics: Firmware Pack I - 32 characters per line, 16 lines in 2 colors per character with inverse video (May be mixed with semigraphics on a character-by-character basis.).

Firmware Pack II - 42 characters per line, 24 lines of 96 upper and lower case characters with descenders, and inverse video (May be mixed with any graphics mode.).
- Semigraphics: 64 columns by 32 rows in 8 colors, or 64 columns by 48 rows in 8 colors (May be mixed with alphanumerics on a block-by-block basis.).
- Full Graphics: Software selectable display densities are 64x64, 128x64, 128x96, 128x192 in 2 sets of 4 colors, and 256x192 in 2 sets of 1 color.
- Firmware Functions: Firmware Pack I Standard Functions -

Clear screen, change mode, plot point, draw line,
alphanumerics/semigraphics driver, read/write
screen.

- Power Requirements: +8V @ 1.9 Amps Max
+16V @ 300 mA Max
-16V @ 100 mA Max
- Temperature: 0-55°C.

3.0 ASSEMBLY PROCEDURE

3.1 Construction

3.1.1 Tools

While assembling your color graphics board, a clean, well-lighted work area is a must. Tools which you will need are:

- Soldering Iron
- Solder
- Needle nosed pliers
- Small diagonal cutters

3.1.2 Soldering

When assembling electronic components or equipment, it is essential to exercise the "art" of soldering. If all of the connections are properly soldered, the product should work properly the first time power is applied. A hasty and/or poor job of soldering can mean endless hours trying to locate a short circuit or intermittent connection.

3.1.2.1 Soldering Procedure (Figure 1)

- Touch tip of soldering iron to joint until heated.
- Touch end of soldering roll onto heated joint. Allow only 1/8" of solder to melt onto joint.
- The melted solder appears wet and shiny and will flow evenly and completely around the joint to be soldered.
- Remove the soldering iron as soon as both surfaces have been wetted.
- Wipe tip of soldering iron clean with a wet sponge.
- The whole soldering procedure should only take 2-3 seconds to complete.

3.1.2.2 Soldering Tips

- Use a low wattage soldering iron (25 watts maximum) with a small, chisel-shaped tip. Avoid the use of soldering guns.

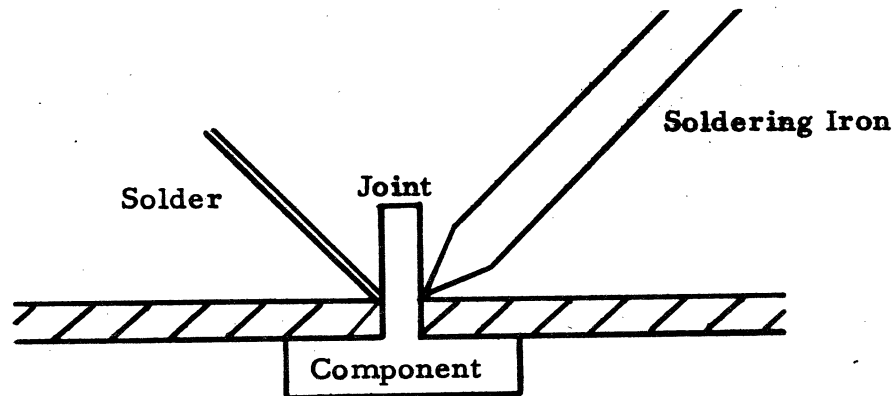


Figure 1 - Soldering Procedure

- Use 60/40 tin/lead solder only.
- Solder neat and rapidly.
- Don't press soldering iron onto the traces and pads. This may cause traces and pads to lift from the board.
- Use a minimum amount of solder. Too much solder will short circuit the bottom of the board, or flow through the holes and short circuit the top of the board.
- Always inspect the board when completed.

3.1.2.3

Soldering Precautions/Problems

- **Excess Solder** - Too much solder can cause short circuits on the bottom of the board, or flow through the holes and short circuit the top of the board.
- **Excess Heat** - Too much heat can cause traces or pads to lift from the board and/or the board base material will begin to turn brown.
- **Cold Solder Joint** - This is caused when not enough heat is applied from the soldering iron causing bad solder connections. Cold solder joints are characterized by a dull, lumpy or balled appearance (Figure 2).

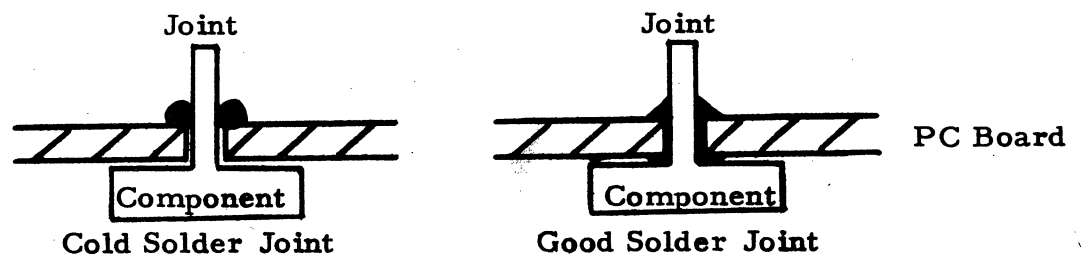


Figure 2 - Good vs. Bad Solder Joint

- Solder Bridges - This is caused from excess solder bridging two or more traces together. Solder bridges are caused by too much solder, soldering too quickly, or too big a soldering iron.

3.1.2.4 Soldering/Assembly Aids

To aid in assembly, the printed circuit board has a solder mask. A component placement layout is also silk screened onto the component side of the PC board.

3.2 Assembly Precautions

- Do not insert or remove your CGS-808 from the computer while the power is turned on.
- Do not insert or remove IC's from the board while the power is turned on.
- Be sure the +5V, -5V, and +12V regulators are generating a +5V, -5V, and +12V output voltage, respectively, before installing any IC's.
- Be careful to insert all IC's in correct positions and with the correct orientation (Figure 3).

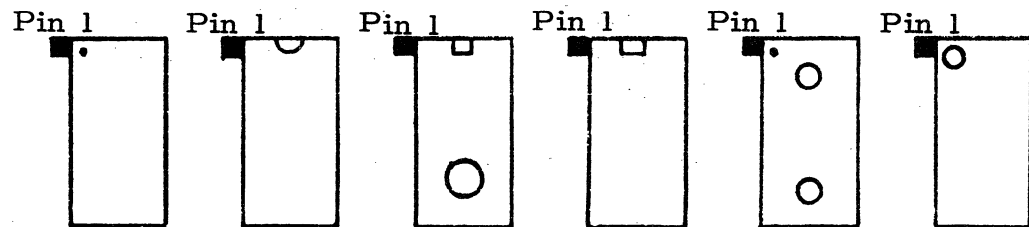


Figure 3 - IC Pin 1 Orientation

- Be careful to insert the electrolytic and tantalum capacitors correctly. Due to polarity, capacitors must be inserted with the positive end oriented correctly (Refer to silk screen legend on PC board and/or the Assembly Drawing located in Appendix E).

3.3 Assembly Procedure

3.3.1 Inspection

- Check the printed circuit board carefully for flaws. Inspect closely for any shorts between traces. Shorts between traces are nearly impossible to locate after the PC board is assembled, especially if they fall underneath

a socket and/or IC.

3.3.2 Board Orientation

Throughout the Assembly Procedure section, the board will be referred to assuming the reader is facing the component side of the board so that the integrated circuit numbers (U numbers) are readable. The regulator and heat sink section is on the left hand edge of the board with the 100 pin edge connector running along the bottom of the board.

3.3.3 Component Insertion

3.3.3.1 Sockets

3.3.3.1.1 Soldering Procedure for Sockets

There are several ways to insert and solder sockets, but Biotech Electronics uses and recommends the following procedure:

- Insert each socket, one at a time, in the designated position.
- After each socket is inserted into the PC board, turn the PC board over and bend two leads of the socket against the PC board so that the socket will stay in the proper position (i.e. on 16 pin socket, bend pins 8 and 16).
- Solder two bent leads only.
- Turn the PC board over and check to see if the socket is flush against the PC board. If not, re-heat both leads and push the socket flush against the PC board.
- Solder the remaining leads.

3.3.3.1.2 Socket Insertion

Install and solder the forty-seven sockets following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check

(/)

- Install and solder the two 40 pin sockets at the following locations: U12, U29.

Check

- () ● Install and solder the two 24 pin sockets at the following locations: U32, U33.
- () ● Install and solder the eight 20 pin sockets at the following locations: U9, U10, U28, U39, U41, U42, U43, U44.
- () ● Install and solder the fifteen 18 pin sockets at the following locations: U3, U4, U5, U6, U7, U8, U13, U14, U15, U16, U17, U18, U19, U30, U31.
- () ● Install and solder the six 16 pin sockets at the following locations: U2, U20, U27, U34, U37, U48.
- () ● Install and solder the fourteen 14 pin sockets at the following locations: U1, U21, U23, U24, U25, U26, U35, U38, U40, U45, U46, U47, J3, J4.

3.3.3.2 Resistors

Install and solder the fourteen resistors following the silk screen legend and/or the Assembly Drawing located in Appendix E. Be sure to wear eye protection when cutting the resistor leads. Proceed as follows:

<u>Check</u>	<u>Resistor Value</u>	<u>R Number</u>	<u>Color Code</u>
()	47 ohms	R8	Yellow/Violet/Black
()	75 ohms	R2	Violet/Green/Black
()	330 ohms	R4	Orange/Orange/Brown
()	360 ohms	R1	Orange/Blue/Brown
()	3.3K ohms	R3, R6, R7	Orange/Orange/Red
()	3.9K ohms	R5	Orange/White/Red
()	5.6K ohms	R9	Green/Blue/Red
()	12K ohms	R13	Brown/Red/Orange
()	51K ohms	R14	Green/Brown/Orange
()	100K ohms	R11, R12	Brown/Black/Yellow

<u>Check</u>	<u>Resistor Value</u>	<u>R Number</u>	<u>Color Code</u>
()	2.2K ohms (7 Resistor SIP)	R10	---

3.3.3.3 Capacitors

Install and solder the thirty capacitors following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

<u>Check</u>	<u>Capacitor Value</u>	<u>C Number</u>
()	.001mfd (Ceramic)	C6
()	.1mfd (Ceramic)	C3, C7, C9, C11, C15, C16, C17, C18, C21, C22, C23, C24, C25, C26, C27, C29, C31
()	3.3mfd (Tantalum Dipped)	C12, C13, C20, C30
()	10mfd (Tantalum Dipped)	C1
()	22mfd (Tantalum Dipped)	C2, C5, C10, C14, C28
()	20pf (Ceramic)	C19
()	47pf (Ceramic)	C8
()	9-35pf (Ceramic Trimmer Capacitor)	C4

NOTE: C28, C29 and C30 required only if using -12V for expansion port.

3.3.3.4 Regulators/Heat Sinks

Install and solder the regulators and heat sinks following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check

- () • Install the 5V positive regulator (U11/LM323K-5) so that the following sequence of hardware results from bottom to top: 6-32 small pan hex nut, PC board, heat sink, 5V regulator, 6-32 small pattern lock washer, 6-32x1/4"

Check

pan head screw. Tighten the bolt, then solder the regulator leads.

- () ● Insert and solder the -5V regulator (U22/79L05) with the flattened edge of the regulator facing the bottom of the board (S-100 edge connector).

- () ● Insert and solder the -12V regulator (U49/79L12) with the flattened edge of the regulator facing the bottom of the board (S-100 edge connector).

NOTE: U49 required only if using -12V for expansion port.

- () ● Bend down the three leads of the 12V positive regulator (U36/7812) 90° so that the leads fit into the correct holes while the bolt holes line up. Do not solder yet.
- Install the 12V regulator so that the following sequence of hardware results from bottom to top: 6-32 small pan hex nut, PC board, 12V regulator, 6-32 small pattern lock washer, 6-32x1/4" pan head screw. Tighten the bolt, then solder the regulator leads.

3.3.3.5 Semiconductors

Check

- () ● 2N2222 Transistor (Q1 and Q2) - Insert and solder the transistors with the tab pointing toward the top of the PC board (as indicated by the tab on the silk screen legend).
- () ● 3.579545 Color Burst Crystal (Y1) - Bend the top two leads 90° so that the leads fit into the correct holes. Insert and solder into the PC board.
- () ● 1N4001 Diode (D1) - Insert and solder the 1N4001 diode such that the band faces the right hand side of the PC board.
- () ● 1N914 Diode (D2) - Insert and solder the 1N914 diode such that the band faces the top of the PC board.

3.3.3.6 Miscellaneous Components

Install and solder the three remaining components following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check

- () ● Insert and solder the 2 pin male molex connector (J2) with the connector pointing toward the top of the PC board.
- () ● Insert and solder the 20 pin 3M connector (J1) with the connector pointing toward the top of the PC board.

NOTE: J1 required only if using RBY Adapter.

- () ● Insert and solder the 6 position dip switch (SW1) as follows (Figure 4):

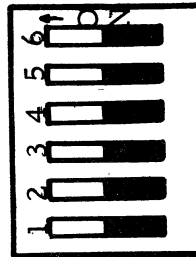


Figure 4 - SW1 Orientation

3.3.4 Voltage Check

- Plug the PC board into the computer.
- Apply power to the PC board. Keep hands and face away from the component side of the PC board.
- Check for +5VDC $\pm 10\%$ at the positive terminal of C2.
- Check for +12VDC $\pm 10\%$ at the positive terminal of C14.
- Check for -5VDC $\pm 10\%$ at the negative terminal of C10.
- Check for -12VDC $\pm 10\%$ at the negative terminal of C28.

3.3.5 Integrated Circuits

3.3.5.1 Integrated Circuit Insertion Tips

- Do not insert IC's with the power on.
- Be sure all IC's are in the correct position and with the

correct orientation (Figure 3). Pin 1 is designated by a white dot adjacent to the upper left hand corner of each IC location.

- Be sure all leads are straight and parallel. If not, gently straighten and align the pins with a pair of needle nosed pliers.
- If the IC leads are wider than the IC socket holes making insertion difficult, close the rows of pins slightly until they are aligned with the IC socket holes. Close the row of pins uniformly by placing the IC on its side on a flat surface, so that one row of pins is flat against the surface (Figure 5).

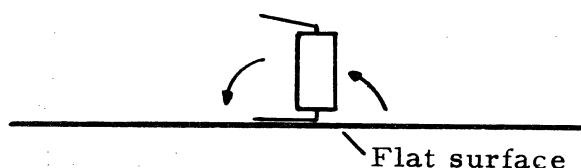


Figure 5 - IC Pin Alignment

Push the row of pins against the flat surface until the pins are vertical to the IC package. Repeat the process to the second row of pins.

- Be sure to handle static sensitive IC's carefully. Do not handle unnecessarily. When installing static sensitive IC's, make sure the IC's, the PC board and your body are grounded.
- If an IC must be removed from the socket, do so carefully so that the pins will not be bent during removal. Remove by gently prying, with a screwdriver, a little bit at a time at each end.

3.3.5.2 Integrated Circuit Insertion

Insert the nineteen static sensitive IC's following the silk screen legend and/or the Assembly Drawing located in Appendix E. Follow the static sensitive insertion tips above. Proceed as follows:

<u>Check</u>	<u>U Number</u>	<u>IC</u>
()	U1	MC1372
()	U12	MC6847

<u>Check</u>	<u>U Number</u>	<u>IC</u>
()	U29	8085
()	U32	2708 (FPI)

NOTE: Install Jumpers W3 and W5
for Firmware Pack I.

()	U3, U4, U5, U6, U7, U8, U13, U14, U15, U16, U17, U18, U19, U30, U31	2114
-----	---	------

Insert the remaining twenty-five IC's following the silk
screen legend and/or the Assembly Drawing located in Appendix E.
Proceed as follows:

<u>Check</u>	<u>U Number</u>	<u>IC</u>
()	U23, U38	74LS00
()	U25, U45	74LS04
()	U24, U47	74LS32
()	U21, U26, U35	74LS74
()	U46	74LS125
()	U2, U20, U34, U48	74LS155
()	U40	74LS243
()	U28	74LS244
()	U41	74LS245
()	U27	74LS367
()	U9, U10, U39, U42, U43, U44	74LS374
()	U37	8131

4.0 THEORY OF OPERATION (Figure 12)

4.1 Color Video Display Generator (VDG)

The heart of the CGS-808 is the Motorola MC6847 Video Display Generator, or VDG (U12). The VDG generates the addresses for the display memory and converts the data to obtain the proper signals, chroma bias, R-Y and B-Y, to the MC1372 Color Encoder (U1). All timing and control is done within the VDG. The MC1372 (U1) generates a 3.58MHz color frequency clock which the VDG uses to generate timing for horizontal sync, horizontal blank, field sync, vertical blank and the dot oscillator. The VDG is designed to produce an NTSC composite video signal. For a detailed description of the MC6847 VDG, refer to Appendix G (Motorola Data Sheet).

The mode control lines of the VDG allow eleven modes of operation. They are divided into three types:

Alphanumeric (1) - The VDG has an internal character generator ROM which accepts a six bit ASCII code, D0-D5. This mode can display 512 characters in a 32 characters per line by 16 line format. The characters are displayed as a 5x7 character matrix in an 8x12 dot matrix. The color set select is controlled by bit D11, and the inverse video is controlled by bit D7 (See Figure 6).

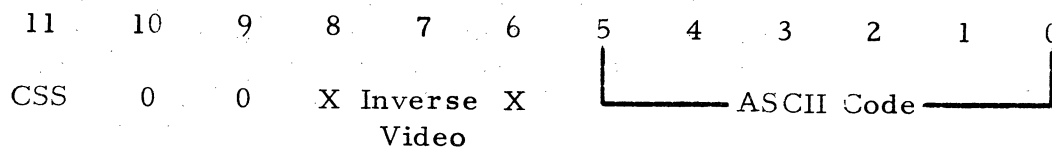


Figure 6 - Alphanumeric Color Set Select

Each character can be programmed for one of two colors (D11 = 0 is green, D11 = 1 is orange). The character color may be inverted by D7 (If D11 (CSS) = 0, then D7 = 0 is a green character on a black background; D7 = 1 is a black character on a green background). See Motorola Data Sheet in Appendix G.

Semigraphics (2) - There are two semigraphic modes: semigraphics-4 and semigraphics-6. In semigraphics-4, each 8x12 dot matrix is divided into four blocks. There are 64 columns by 32 rows of display elements. Each character of four blocks can be programmed to one of eight colors (See Figure 7).

11	10	9	8	7	6	5	4	3	2	1	0
X	1	0	X	X	C2	C1	C0	L3	L2	L1	L0

L3	L2
L1	L0

Figure 7 - Semigraphics-4

In semigraphics-6, each 8x12 dot matrix is divided into six blocks. There are 64 columns by 48 rows of display elements. Each character of six blocks can be programmed to one of eight colors (See Figure 8).

11	10	9	8	7	6	5	4	3	2	1	0
C2	1	1	X	C1	C0	L5	L4	L3	L2	L1	L0

L5	L4
L3	L2
L1	L0

Figure 8 - Semigraphics-6

Graphics (8) - The eight graphic modes are sub-divided into four 2-color graphic modes or four 4-color graphic modes. The graphic modes are selected by GM0, GM1 and GM2 of the mode port. Two possible color sets are available and may be selected through the use of the color set select bit (CSS), D4 of the mode port (See Figure 9).

7	6	5	4	3	2	1	0
EN FW	EN HW	EXT VID	CSS	$\overline{A/G}$	GM2	GM1	GM0

Figure 9 - Mode Port Bits

The 4-color graphic modes use 2 bits of RAM per pixel where the 2 bits decode into one of four colors, while the 2-color graphic modes use a single bit in RAM per pixel. These graphic modes allow display densities ranging from 64x64 to 256x192 using 1K of memory. For a complete description of each mode, refer to Appendix G (Motorola Data Sheet).

4.2

Screen Refresh Memory

The CGS-808 has 6 1/2K bytes of screen refresh memory. The VDG address lines (A0-A12) constantly scan the screen refresh memory. The data from this memory is processed by the VDG and transformed into luminescence Y (Pin 28 of U12/MC6847), and color outputs 0A and 0B (Pins 10 and 11 of U12/MC6847). The screen refresh memory is shared between the on-board 8085 processor and the VDG. The processor can read or write to any location in the refresh memory. The VDG uses a different amount of memory depending on the mode (Refer to page G-8 in Appendix G). The full graphic modes (0-7) use from 1K to 6K bytes of the screen refresh memory; the alphanumeric/semigraphics mode uses only 512 words.

The alphanumeric/semigraphics mode uses 11 bits of data from the 8085. This data is divided into two parts: the full word data (FWD), 8 bits from U3 and U4 (2114); and the half word data (HWD), 3 bits from U13 (2114). The half word data is used to program the mode bits CSS, A/S and INT/EXT on a character by character basis. These extra 3 bits allow the software to mix the alphanumerics, semigraphics-4 and semigraphics-6 on the same display. The CSS, or color select signal, is multiplexed between the mode port (Pin 12 of U39/74LS367) and the half word memory (Pin 14 of U13/2114). In the alphanumeric/semigraphics mode, the memory data bit D3 (Pin 14 of U3/2114) of the half word memory becomes the CSS bit. To program in the alphanumeric/semigraphics mode, both the HWD and the FWD must be specified; however, in the full graphic modes only the FWD is used. The mode port bits 6 and 7 (Pins 16 and 19 of U39/74LS374) are used to enable either the HWD or FWD. These 2 bits should never be enabled at the same time. When reading or writing to the HWD, only 3 bits are used and the rest can be ignored (See Figures 10 and 11).

HWD							
8	7	6	5	4	3	2	1
X	X	X	X	D11	D10	D9	D8
			*	CSS	A/S	INT/ EXT	X
FWD							
8	7	6	5	4	3	2	1
D7	D6	D5	D4	D3	D2	D1	D0
Alphanumeric/Semigraphic Data							

X = Don't Care

Figure 10 - HWD/FWD Bit Definition

D10	D9	
A/S	INT/EXT	
0	0	Alphanumeric
0	1	NOT USED
1	0	Semigraphics-4
1	1	Semigraphics-6

Figure 11- HWD Mode Selection

The screen refresh memory can be accessed by the 8085 microprocessor only during a time when the MC6847 VDG (U12) is not in an active display region (i.e. blanking during a horizontal or vertical retrace). The "D" type flip-flop (U26/74LS74) synchronizes the 8085 processor memory during read and write operations with the horizontal ($\overline{HS}$ - pin 38 of U12/MC6847) or vertical ($\overline{FS}$ - pin 37 of U12/MC6847) sync of the MC6847. When the screen refresh memory is not selected by the processor, the Q output (Pin 5 of U26/74LS74) is high causing the ready line of the 8085 to be held high (Pin 35 of U29/8085). The processor can only enter a wait state while attempting to access the screen refresh memory.

When the 8085 accesses the refresh memory, a memory select signal ($\overline{MS}$ active low) is generated by U20 (74LS155). When $\overline{MS}$ (Pin 12 of U20/74LS155) and the D input (Pin 2 of U26/74LS74) are low, and the Q output (Pin 5 of U26/74LS74) is high and pin 1 of U38 (74LS00) is high, causing pin 3 of U38 (74LS00) to go low placing the 8085 in a wait state. The falling edge of $\overline{HS}$ (Pin 38 of U12/MC6847) causes the Q output (Pin 5 of U26/74LS74) to go low, and pin 3 of U38 (74LS00) to go high taking the processor out of a wait state. Pin 8 of U23 (74LS00) will also go low causing the MC6847 to tri-state its address bus and enable U27 (74LS367), U28 (74LS244), U40 (74LS243) and U41 (74LS245), the address and data buffers. The processor is then allowed to read or write into the screen refresh memory without causing snow on the display.

4.3 8085 Microprocessor

The on-board microprocessor (U29/8085) executes the programs in Firmware Pack I and II to provide the intelligence for plotting points, drawing lines, circles, etc. The 8085 is 8080 software compatible allowing the user to develop his/her own graphic driver subroutines. Components C20, D2 and R14 provide the power-on-clear for the 8085. Jumper W1 allows the external clear signal, pin 54 of the S-100 bus, to clear the 8085 processor. Jumper W2 allows the PRESET signal, pin 75 of the S-100 bus, to clear the 8085 microprocessor.

The microprocessor clock for the 8085 is controlled by adjusting R13. Increasing R13 will slow down the processor. R13 can

range from 12K - 24K ohms. The processor can easily be modified for crystal control by replacing R13 with a 6.144MHz small case crystal.

4.4 Processor Memory

The CGS-808 has three blocks of memory: 6 1/2K bytes of screen refresh memory, 1K byte of RAM for the parameter and data base storage, and up to 4K bytes of EPROM storage for the firmware subroutines.

The 1K byte of parameter RAM consists of U30 and U31, two 2114 low power static RAMs. All memory decoding is done by U20 (74LS155), a 3 to 8 line decoder. The 1K byte of RAM starts at 4000H through 43FFH.

Firmware Pack I is stored on a 2708 1K byte EPROM, and is installed in socket U32 with jumpers W3 and W5 to connect the -5V and +12V supplies. Socket U32 is set at address 0000H. Firmware Pack II is a 2708 1K byte EPROM, and is installed in socket U33 with jumpers W8 and W10 installed. Socket U33 is set at address 2000H. Either U32 or U33 can be configured for 2708's or 2716's (Only single supply 2716's can be used).

4.5 S-100 I/O Port

The CGS-808 uses two I/O ports for all data transfer to the on-board processor. The port address is placed on the lower order address lines (A0-A7) with an SOUT or SINP, and either PWR or PDBIN (U45/74LS04, U47/74LS32) from the host CPU will generate an INPUT or OUTPUT signal to U48 (74LS155). If address lines A2-A7 compare with the switch settings of SW1, then U37, an 8131 6 bit comparator, will enable U48, a dual 2 to 4 line decoder (74LS155). The generated INPUT or OUTPUT signal from U45 (74LS04) and U47 (74LS32) will select either the lower or upper 4 bits of U48 (74LS155) and decode which I/O port will be selected.

SW1 can select any I/O port on any four I/O port address boundaries. All switches "on" will select port 0 and 1. The most significant bit is at the top of SW1.

Full handshaking is provided for each I/O port (See System Configuration in Appendix A).

4.6 Expansion Port

The CGS-808 has the provision for one 8 bit parallel input port and one 8 bit parallel output port. Full handshaking is provided.

The parallel input consists of J3 (14 pin socket), U9 (74LS374) and pin 3 of U21 (74LS74). When data is valid on the data in, bit DI0-DI7 of J3, and the strobe goes from low to high (Pin 1 of J3); the data will be latched in the expansion port (U9/74LS374). The interrupt flip-flop (Pin 5 of U21/74LS74) will be set causing the processor to vector to location 34 Hex (RST 6.5) and read the expansion input port 02. An output to port 03 in the software will reset the interrupt flip-flop (U21/74LS74).

The parallel output consists of J4 (14 pin socket), U10 (74LS374) and pin 11 of U21 (74LS74). The 8085 processor will output the expansion port data to port 02. The external peripheral must supply a low to high signal (Pin 1 of J4) to enable the data out bits, DO0-DO7. The strobe will cause the interrupt flip-flop (Pin 9 of U21/74LS74) to be set and vector the program to location 2C Hex (RST 5.5). An output to port 03 in the software will reset the interrupt flip-flop (Pins 1 and 13 of U21/74LS74).

Two instructions of the 8085 are used to set and test the interrupt mask (SIM instruction, OP-Code 30 Hex to enable RST 7.5, 6.5, 5.5, the accumulator, must be 18 before the SIM instruction is executed):

FB	EI	Enable Interrupts
3E18	MVI A, 18H	Reset Interrupt Mask
30	SIM	7.5, 6.5, 5.5

4.7 Color Encoding

The four outputs from the VDG (Y, R-Y, B-Y and BIAS) drive the MC1372 modulator chip (U1). The MC1372 is not used to generate an RF signal, but rather to combine Y, R-Y and B-Y to provide a composite video signal. The MC1372 generates a 3.579545MHz color sub-carrier for the VDG. By adjusting the variable trimmer capacitor (C4), the sub-carrier frequency is changed causing the color to change slightly. The trimmer capacitor should be adjusted so on power up, the display is in color.

The composite video is configured for a non-inverted video. The polarity of the video is controlled by the direction of the diode D1. Pins 13 and 14 of the MC1372 can be reversed to produce an inverted video signal.

The luminescence to chromanescence ratio (L:C) may be modified by changing R4 (330 ohm resistor). The gain for an unmodified L:C (Ao) is typically 0.883 or -16dB. The modified L:C will be governed by the equation $A_o (1 + R4/800)$ for equal amplitude input signals.

If the CGS-808 is to be used with a black and white monitor only, either C7 (.1mfd) or R4 (330 ohms) should be removed. This will eliminate the chromanescence signal.

Transistor Q1 is a common collector amplifier with a gain of approximately 22. By changing R6 (3.3K ohms), the gain can be adjusted to vary the peak-to-peak amplitude of the composite video out.

Transistor Q2 is a common emitter voltage follower with a gain of 1. Transistor Q1 provides buffering to produce an NTSC compatible signal with a 75 ohm impedance.

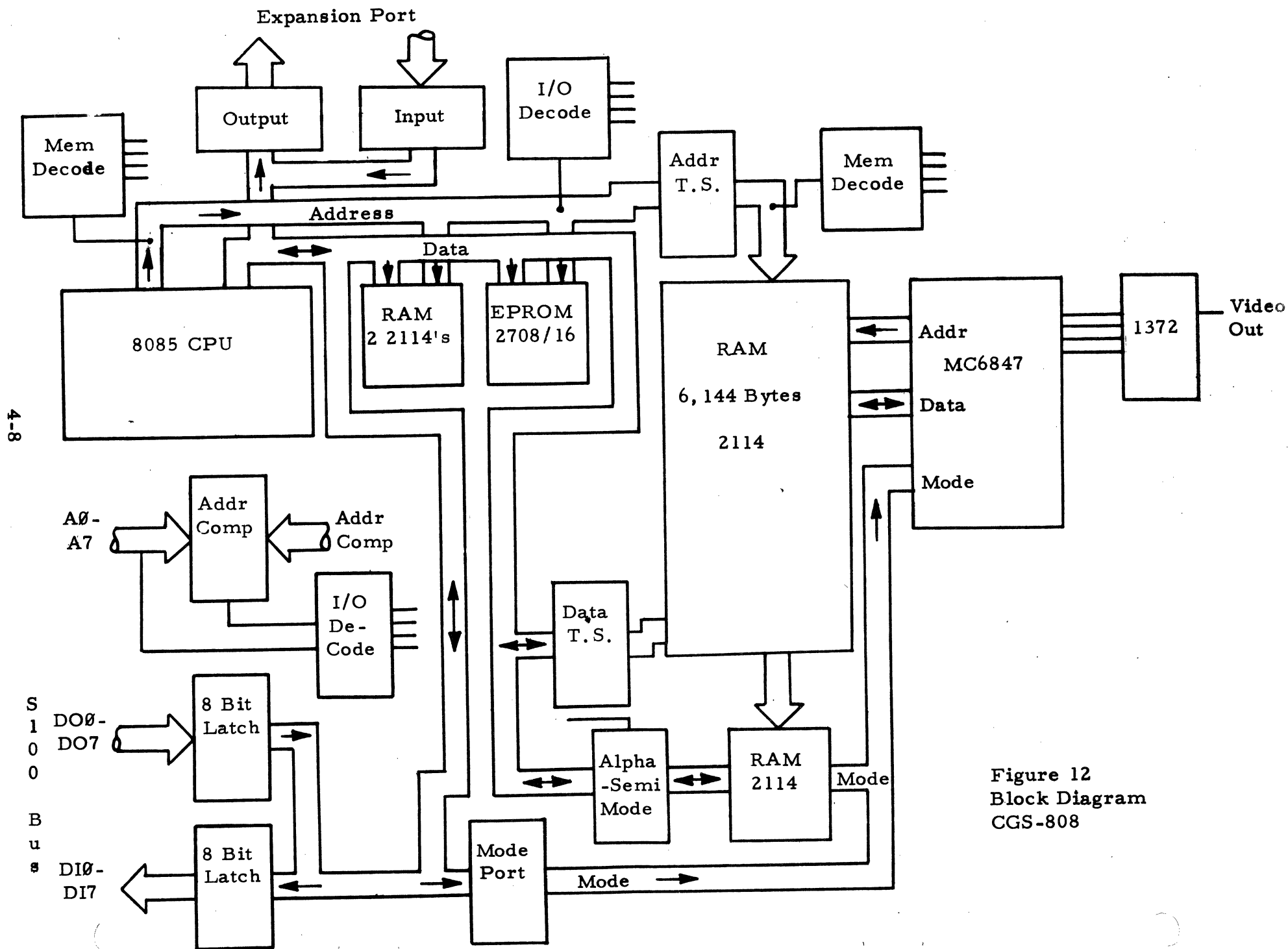


Figure 12
Block Diagram
CGS-808

I/O Ports - On-Board

Input Ports With Respect To 8085:

- 0 S-100 Data Input
- 1 Status Input
- 2 Expansion Port Input

Output Ports With Respect To 8085:

- 0 S-100 Data Output
- 1 Mode Output
- 2 Expansion Port Output

Status Bit Definition - Input Port 1:

- Bit 0 S-100 Output Data Status
 - 1 = Data Not Taken (Busy)
 - 0 = Data Taken (Done)
- Bit 7 S-100 Input Data Status
 - 1 = No Data In Register
 - 0 = Data Ready

Mode Port Bit Definition - Output Port 1:

- Bit 7 +Enable Full Word Memory
- Bit 6 +Enable Half Word Memory
- Bit 5 +Enable External Video
- Bit 4 Color Select Signal (CSS)
- Bit 3 A/G (0 = Alphanumerics,
 - 1 = Graphics)
- Bit 2 GM2 (Graphics Mode)
- Bit 1 GM1 (Graphics Mode)
- Bit 0 GM0 (Graphics Mode)

I/O Ports - S-100

Input Ports With Respect To S-100 Bus:

- 0 Data Input
- 1 Status Input

Output Ports With Respect To S-100 Bus:

- 0 Data Output
- 1 Initiate (Data is don't care)

Status Bit Definitions:

- Bit 0 Output Data
 - 1 = Data Not Taken (Busy)
 - 0 = Data Taken (Done)
- Bit 7 Input Data
 - 1 = No Data In Register
 - 0 = Data In Register

SW1 - Address Compare Switches

SW1-1 = Address Bit 2 - LSB at Bottom of Board

SW1-6 = Address Bit 7 - MSB at Top of Board

Open = Off = 0; Closed = On = 1

SW1-6	On	On	On	Off	Off
SW1-5	On	On	On	On	On
SW1-4	On	On	On	On	Off
SW1-3	On	On	On	On	On
SW1-2	On	On	Off	On	On
SW1-1	On	Off	Off	On	On

Port	00H	04H	06H	80H	A0H
------	-----	-----	-----	-----	-----

Memory Map - On-Board

0000H	[	Firmware Pack I
03FFH		2708
07FFH		2716
2000H	[	Firmware Pack II
23FFH		2708
27FFH		2716
4000H	[	Parameter - RAM
43FFH		2114
6000H	[	Screen Refresh RAM
61FF		Half Word
7DFF		

EPROM Configuration

Socket U32

- 2708 Install Jumpers W3 and W5*
2716 Install Jumpers W4 and W6

Socket U33

- 2708 Install Jumpers W8 and W10**
2716 Install Jumpers W7 and W9

*Firmware Pack I

**Firmware Pack II

Power On - Reset

PRESET Pin 75 Install Jumper W2

EXTCLR Pin 54 Install Jumper W1

8085 Interrupts

<u>Priority</u>	<u>Restart</u>	<u>Addr Dec</u>	<u>Hex</u>
Highest	5.5	28	2C Exp Port Output Data Taken
	6.5	42	34 Exp Port Input Data Available
	7.0	56	38 Reset Required
Lowest	7.5	60	3C Execute OP-Code
			Port 1 - S-100

APPENDIX B

Troubleshooting

The first step to fixing your CGS-808 is to check the obvious. Proceed as follows:

- (a) Check for the proper settings of the dip switch.
- (b) Verify that all IC's are in the correct sockets with pin 1 correctly oriented on all IC's.
- (c) Visually inspect to see that all IC leads are in the sockets, not bent under.
- (d) Verify the output voltages are correct.
- (e) Inspect the solder side of the PC board for solder bridges. Run a sharp knife between traces that look suspicious. A magnifying glass is a must.
- (f) Check for proper jumper installation.

Having done all of the above and the board still does not work, then there is most likely a bad device. Proceed as follows:

- (a) If you have a problem with the screen refresh memory:

- (1) Check U23 (74LS00), U25 (74LS04), U26 (74LS74), and U38 (74LS00) for the $\overline{MS}$ signal, and pin 12 of U12 (MC6847) going low.
- (2) Check U2 (74LS155), U27 (74LS367), and U28 (74LS244) for shorts and proper operation.

- (b) If you have a problem with the screen refresh data (consisting of missing bits):

- (1) Check U3 through U8 (2114) for lower 4 bits of data.
- (2) Check U14 through U19 (2114) for upper 4 bits of data.
- (3) Check U41 (74LS245) for proper direction of data flow.
- (4) Check U23 (74LS00), U24 (74LS32) and U40 (74LS243) half word data.

Troubleshooting (Con't.)

(c) If the mode does not change:

- (1) Check U39 (74LS374) for the appropriate bits to be set.
- (2) Check pin 11 of U39 (74LS374) for a clock pulse.
- (3) Check U38 (74LS00) for the proper CSS bit.
- (4) Check U13 (2114) and U40 (74LS243) for the proper half word mode bits.

(d) If the memory cannot be read or written into:

- (1) Verify the appropriate mode bit is set: bit 7 for full word enable, bit 6 for half word enable (not both).
- (2) Check pin 8 of the 2114 memory for proper 1K bank select.
- (3) Check pin 10 of the 2114 memory for a low write signal.
- (4) Check U40 (74LS243) or U41 (74LS245) for proper direction of data flow: U41 - pin 19 low equals tri-state enabled; U41 - pin 1 high equals data read; U41 - pin 1 low equals data write.
- (5) Verify pin 12 of U12 (MC6847) is low.
- (6) Verify that either $\overline{HS}$ or $\overline{FS}$ is low during a read or write.

(e) If the Firmware Pack I does not run:

- (1) Check if the 2708 EPROM has a program stored in it.
- (2) Check for a reset out signal at pin 3 of U29 (8085).
- (3) Check for a clock out at pin 37 of U29 (8085) (Should be greater than 350ns period).
- (4) Check the ready signal, pin 35 of U29 (8085), to see if it is high.

Troubleshooting (Con't.)

- (5) Check for the proper jumper positions for U32 (W3 and W5 for a 2708).
- (6) Check for a chip select signal at pin 20 of U32 (2708 EPROM).
- (7) Check for proper operation of U42 (74LS374) and ALE pin 30 of U29 (8085) for lower address bits.
- (8) Check pin 9 of U20 (74LS155) for a chip select signal.

(f) If the S-100 I/O does not work:

- (1) Check SW1 dip switch settings.
- (2) Check the input port (At the dip switch address should be C0 Hex).
- (3) Check pin 9 of U37 (8131) for address compare.
- (4) Check pin 1 of U48 (74LS155) for an output strobe.
- (5) Check pin 15 of U48 (74LS155) for an input strobe.
- (6) Check U48 (74LS155): pin 7 and U43 (74LS374) for data out; pin 6 and U29 (8085) for initiate strobe; pin 9 and U44 (74LS374) for data input; pin 10 and U35 (74LS74), U46 (74LS125) for status.
- (7) Check U34 (74LS155) for data and status strobes.

(g) If the expansion port doesn't work:

- (1) Check pin 1 and 13 of U21 (74LS74) to be high.
- (2) Check pin 5 and 9 of U21 (74LS74) to be low.
- (3) Check pin 1 of U9 (74LS374) for the input strobe.

Troubleshooting (Con't.)

- (4) Check pin 1 of U10 (74LS374) for the output strobe.
- (5) Check to see if pin 5 or 9 of U21 (74LS74) is set high.
- (6) Check pin 1 of U9 (74LS374) or pin 11 of U10 (74LS374) for proper operation.

(h) If there is no picture:

- (1) Check the color clock (Pin 33 of U12/MC6847) with a high impedance scope probe (x10) for a 50% duty cycle at 3.579545MHz (symmetrical wave form). Adjust C4 for the proper signal.
- (2) Check D1 for proper polarity anode at pin 14 of U1 (MC1372).
- (3) Check for a video signal at pin 9 of U1 (MC1372).
- (4) Check for approximately 2VDC at pin 6 of U1 (MC1372).
- (5) Check collector of Q1 (2N2222 transistor) for a composite video signal.
- (6) Check emitter of Q2 (2N2222 transistor) for a 1.0V to 1.5Vpp composite video signal (negative sync).

APPENDIX C

Parts List

Resistors

<u>R Number</u>	<u>Resistor Value</u>	<u>Color Code</u>
R1	360 ohms	Orange/Blue/Brown
R2	75 ohms	Violet/Green/Brown
R3	3.3K ohms	Orange/Orange/Red
R4	330 ohms	Orange/Orange/Brown
R5	3.9K ohms	Orange/White/Red
R6	3.3K ohms	Orange/Orange/Red
R7	3.3K ohms	Orange/Orange/Red
R8	47 ohms	Yellow/Violet/Black
R9	5.6K ohms	Green/Blue/Red
R10	2.2K ohms 7 resistor SIP	---
R11	100K ohms	Brown/Black/Yellow
R12	100K ohms	Brown/Black/Yellow
R13	12K ohms	Brown/Red/Orange
R14	51K ohms	Green/Brown/Orange

Unless otherwise specified, all resistors are 1/4 watt 5%.

Capacitors

<u>C Number</u>	<u>Capacitor Value</u>	<u>Capacitor Type</u>
C1	10mfd	Tantalum Dipped
C2	22mfd	Tantalum Dipped
C3	.1mfd	Ceramic
C4	9-35pf	Ceramic Trimmer Capacitor
C5	22mfd	Tantalum Dipped
C6	.001mfd	Ceramic
C7	.1mfd	Ceramic
C8	47pf	Ceramic
C9	.1mfd	Ceramic
C10	22mfd	Tantalum Dipped
C11	.1mfd	Ceramic
C12	3.3mfd	Tantalum Dipped
C13	3.3mfd	Tantalum Dipped
C14	22mfd	Tantalum Dipped
C15	.1mfd	Ceramic
C16	.1mfd	Ceramic
C17	.1mfd	Ceramic

Parts List (Con't.)

Capacitors (Con't.)

<u>C Number</u>	<u>Capacitor Value</u>	<u>Capacitor Type</u>
C18	.1mfd	Ceramic
C19	20pf	Ceramic
C20	3.3mfd	Tantalum Dipped
C21	.1mfd	Ceramic
C22	.1mfd	Ceramic
C23	.1mfd	Ceramic
C24	.1mfd	Ceramic
C25	.1mfd	Ceramic
C26	.1mfd	Ceramic
C27	.1mfd	Ceramic
C28	22mfd	Tantalum Dipped
C29	.1mfd	Ceramic
C30	3.3mfd	Tantalum Dipped
C31	.1mfd	Ceramic

Semiconductors

<u>Semi Number</u>	<u>Semi Type</u>	<u>Semi Description</u>
D1	1N4001	Diode
D2	1N914	Diode
Q1	2N2222	Transistor
Q2	2N2222	Transistor
Y1	3.579545	Color Burst Crystal

Integrated Circuits.

<u>IC Number</u>	<u>IC Type</u>	<u>IC Description</u>
U1	MC1372	Modulator/Encoder
U2	74LS155	Decoder/Demultiplexer
U3	2114	1KX4 Static RAM
U4	2114	1KX4 Static RAM
U5	2114	1KX4 Static RAM
U6	2114	1KX4 Static RAM
U7	2114	1KX4 Static RAM
U8	2114	1KX4 Static RAM
U9	74LS374	Octal Flip-Flop
U10	74LS374	Octal Flip-Flop
U11	LM323K-5	5V Positive Regulator
U12	MC6847	Video Display Generator

Parts List (Con't.)

Integrated Circuits (Con't.)

<u>IC Number</u>	<u>IC Type</u>	<u>IC Description</u>
U13	2114	1KX4 Static RAM
U14	2114	1KX4 Static RAM
U15	2114	1KX4 Static RAM
U16	2114	1KX4 Static RAM
U17	2114	1KX4 Static RAM
U18	2114	1KX4 Static RAM
U19	2114	1KX4 Static RAM
U20	74LS155	Decoder/Demultiplexer
U21	74LS74	Dual Positive-Edge- Triggered Flip-Flop
U22	79L05	-5V Regulator
U23	74LS00	Quad 2-Input Positive- Nand Gate
U24	74LS32	Quad 2-Input Positive-Or Gate
U25	74LS04	Hex Invertor
U26	74LS74	Dual Positive-Edge- Triggered Flip-Flop
U27	74LS367	Hex Bus Driver
U28	74LS244	Octal Buffer/Line Driver/ Line Receiver
U29	8085	Microprocessor
U30	2114	1KX4 Static RAM
U31	2114	1KX4 Static RAM
U32	2708	EPROM 450ns
U33	2708	EPROM 450ns
U34	74LS155	Decoder/Demultiplexer
U35	74LS74	Dual Positive-Edge- Triggered Flip-Flop
U36	7812	12V Positive Regulator
U37	8131	6-Bit Comparitor
U38	74LS00	Quad 2-Input Positive- Nand Gate
U39	74LS374	Octal Flip-Flop
U40	74LS243	Quadruple Bus Transceiver
U41	74LS245	Octal Bus Transceiver
U42	74LS374	Octal Flip-Flop
U43	74LS374	Octal Flip-Flop
U44	74LS374	Octal Flip-Flop
U45	74LS04	Hex Invertor
U46	74LS125	Quadruple Bus Buffer Gate

Parts List (Con't.)

Integrated Circuits (Con't.)

<u>IC Number</u>	<u>IC Type</u>	<u>IC Description</u>
U47	74LS32	Quad 2-Input Positive-Or Gate
U48	74LS155	Decoder/Demultiplexer
U49	79L12	-12V Regulator

Miscellaneous

<u>Number</u>	<u>Description</u>
J1	20 Pin 3M Connector
J2	2 Pin Male Molex Connector
SW1	6 Positive Dip Switch

<u>Quantity</u>	<u>Description</u>
14	14 Pin Low Profile Socket (Solder Tail)
6	16 Pin Low Profile Socket (Solder Tail)
15	18 Pin Low Profile Socket (Solder Tail)
8	20 Pin Low Profile Socket (Solder Tail)
2	24 Pin Low Profile Socket (Solder Tail)
2	40 Pin Low Profile Socket (Solder Tail)
1	TO-3 Heat Sink
3	6-32x1/4" Pan Head Screw
3	6-32 Small Pan Hex Nut
3	6-32 Small Pattern Lock Washer
1	PC Board
1	Hardware Manual
1	Software Manual

APPENDIX D

Parts List Summary

Resistors

1	47 ohms
1	75 ohms
1	330 ohms
1	360 ohms
3	3.3K ohms
1	3.9K ohms
1	5.6K ohms
1	12K ohms
1	51K ohms
2	100K ohms
1	2.2K ohms 7 resistor SIP

Unless otherwise specified, all resistors are 1/4 watt 5%.

Capacitors

1	.001mfd (Ceramic)
17	.1mfd (Ceramic)
4	3.3mfd (Tantalum Dipped)
1	10mfd (Tantalum Dipped)
5	22mfd (Tantalum Dipped)
1	20pf (Ceramic)
1	47pf (Ceramic)
1	9-35pf (Ceramic Trimmer Capacitor)

Semiconductors

1	3.579545 Color Burst Crystal
2	2N2222 GP NPN Transistor
1	1N4001 Diode
1	1N914 Diode

Integrated Circuits

2	74LS00	Quad 2-Input Positive-Nand Gate
2	74LS04	Hex Invertor
2	74LS32	Quad 2-Input Positive-Or Gate
3	74LS74	Dual Positive-Edge-Triggered Flip-Flop with Preset and Clear
1	74LS125	Quadruple Bus Buffer Gate
4	74LS155	Decoder/Demultiplexer

Parts List Summary (Con't.)

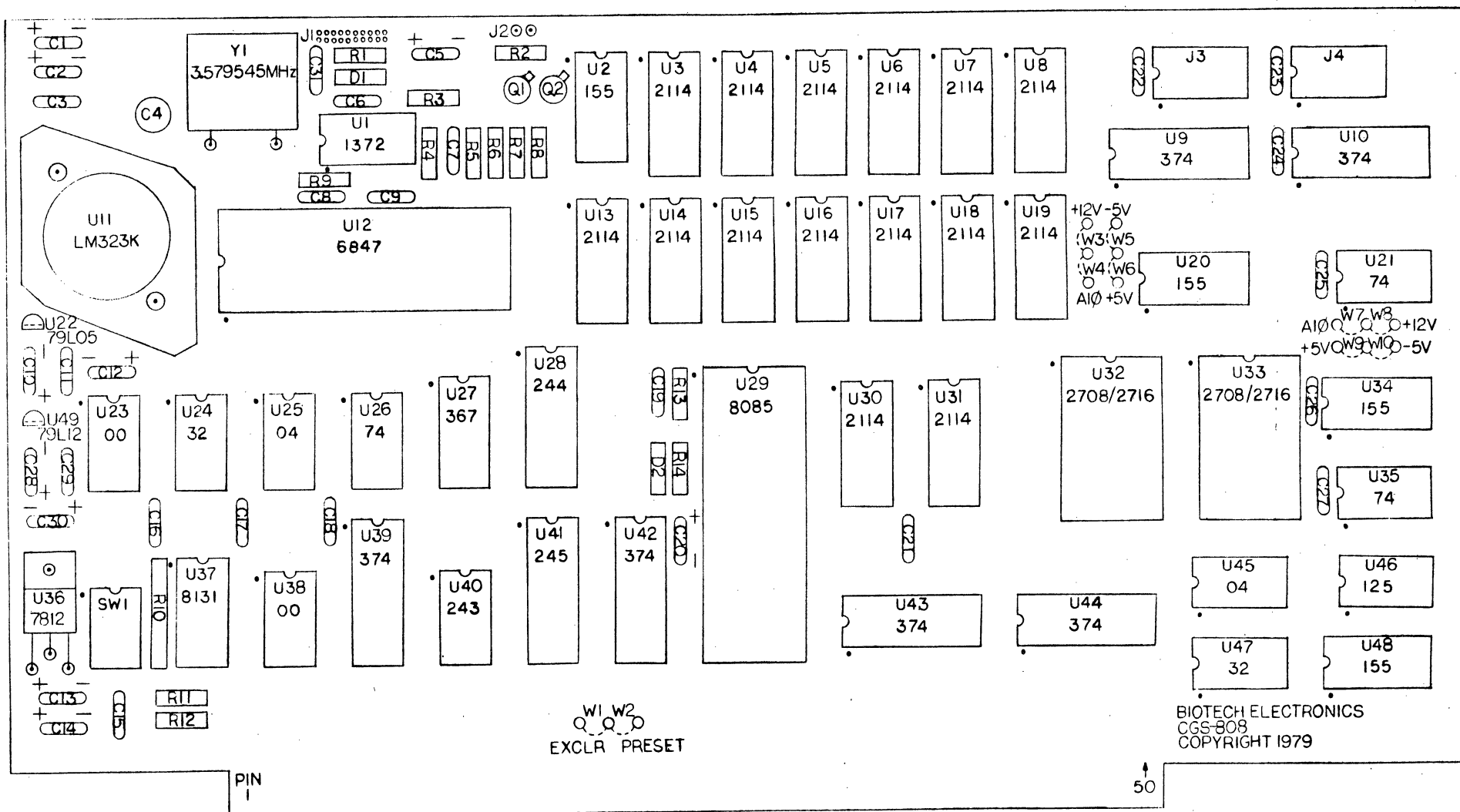
Integrated Circuits (Con't.)

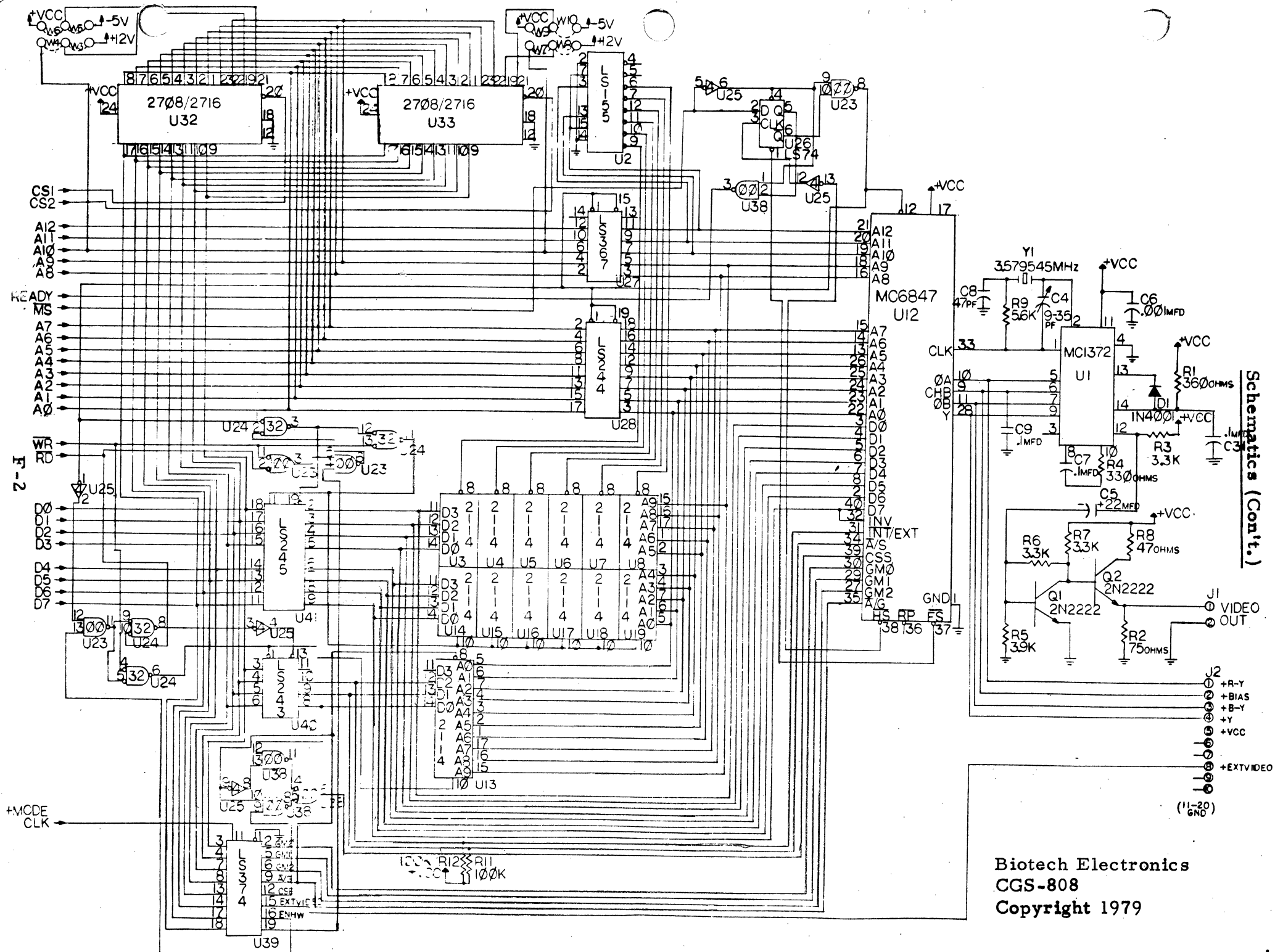
1	74LS243	Quadruple Bus Transceiver
1	74LS244	Octal Buffer/Line Driver/Line Receiver
1	74LS245	Octal Bus Transceiver
1	74LS367	Hex Bus Driver
6	74LS374	Octal Flip-Flop
1	8131	6-Bit Comparator
1	LM323K-5	5V Positive 3 Amp Regulator
1	7812	12V Positive 1 Amp Regulator
1	79L05	-5V 100mA Regulator
1	79L12	-12V 100mA Regulator
15	2114	1KX4 450ns Low Power Static RAM
* 1	2708	EPROM 450ns
* 1	8085	Microprocessor
* 1	MC1372	Modulator/Encoder
* 1	MC6847	Video Display Generator

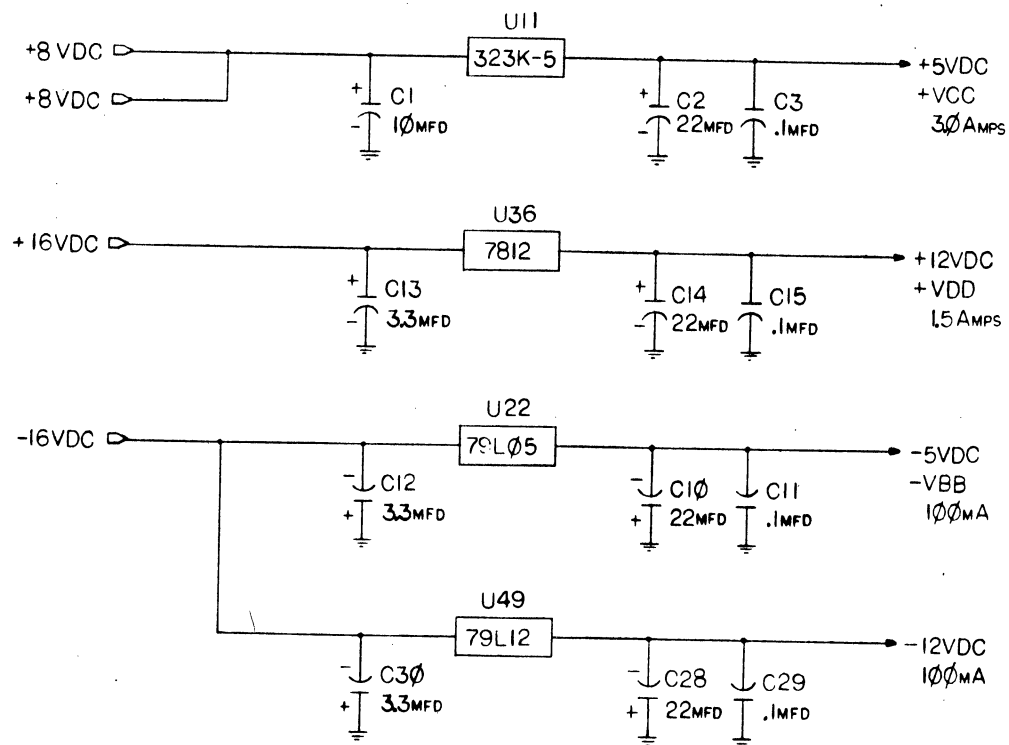
Miscellaneous

14	14 Pin Low Profile Socket (Solder Tail)
6	16 Pin Low Profile Socket (Solder Tail)
15	18 Pin Low Profile Socket (Solder Tail)
8	20 Pin Low Profile Socket (Solder Tail)
2	24 Pin Low Profile Socket (Solder Tail)
2	40 Pin Low Profile Socket (Solder Tail)
1	2 Pin Right Angle Molex Wafer Connector (09-66-1021) KK156
1	2 Pin Molex Crimp Connector (09-50-7021) KK156
2	Molex Crimp Terminal (08-50-0108) KK156
1	20 Pin Right Angle (.1x.1) - AP Products 923872-R
1	6 Position Dip Switch
1	TO-3 - Thermalloy Heat Sink THM6013B
3	6-32x1/4" Pan Head Screw
3	6-32 Small Pan Hex Nut
3	6-32 Small Pattern Lock Washer
* 1	PC Board
* 1	Hardware Manual
* 1	Software Manual

*Supplied with bare "kit" (PC board, Hardware Manual, Software Manual, 8085, MC6847, MC1372, and 2708 with software graphic driver routines).







Schematics (Con't.)

APPENDIX G

Motorola Data Sheet

Advance Information

VIDEO DISPLAY GENERATOR (VDG)

The Motorola MC6847 Video Display Generator (VDG) provides a means of interfacing the Motorola M6800 microprocessor family (or similar products) to a commercially available color or black and white television receiver. Applications of the VDG include video games, bioengineering displays, education, communications and any place graphics are required.

The VDG reads data from memory and produces a composite video signal which will allow the generation of alphanumeric or graphic displays. The generated composite video may be up modulated to either Channel 3 or 4 by using the compatible MC1372 (TV Chroma and Video modulator). The up modulated signal is suitable for application to the antenna of a color TV. A typical TV game is indicated in Figure 1.

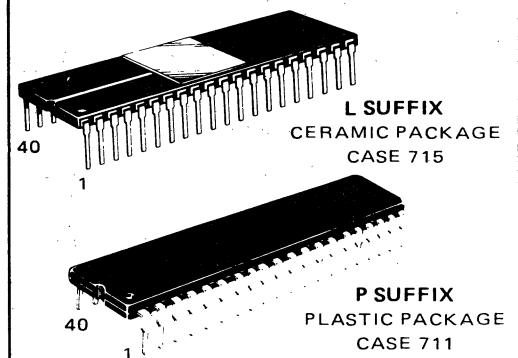
- Generates four different alphanumeric display modes and eight graphic display modes
- Compatible with the M6800 family
- Compatible with the MC1372 modulator
- The alphanumeric modes display 32 characters per line by 16 lines
- An internal multiplexer allows the use of either the internal ROM or an external character generator
- An external character generator can be used to extend the internal character set for "limited graphic" shapes
- A Mask Programmable internal character generator ROM is available on special order (Appendix A)
- One display mode offers 8-color 64 x 32 density graphics in an alphanumeric display mode
- One display mode offers 4-color 64 x 48 density graphics in an alphanumeric display mode
- All alphanumeric modes have a selectable video inverse
- Generates full video signal
- Generates R-Y and B-Y signals for external color modulator
- Full-graphic modes offer 64 x 64, 128 x 64, 128 x 96, 128 x 192, or 256 x 192 densities
- Full-graphic modes allow 2-color or 4-color data structures
- Full-graphic modes use one of two 4-color sets or one of two 2-color sets
- Available in either an interlace mode (NTSC Standard) or a non-interlace mode

MC6847
NONINTERLACE
MC6847Y
INTERLACE

MOS

(N-CHANNEL, SILICON-GATE)

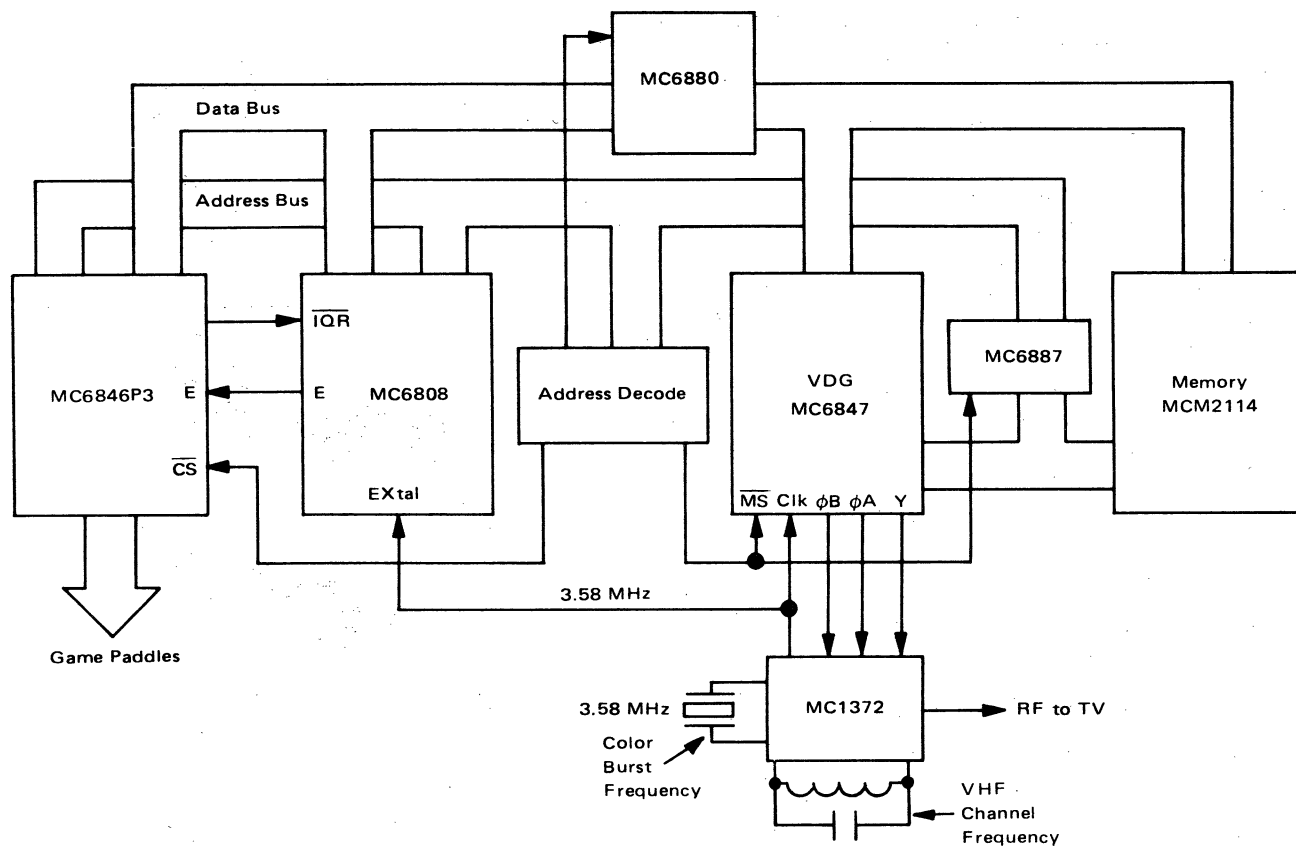
**VIDEO
DISPLAY
GENERATOR**



PIN ASSIGNMENT

1	V _{SS}	DD7	40
2	DD6	CSS	39
3	DD0	HS	38
4	DD1	FS	37
5	DD2	RP	36
6	DD3	A/G	35
7	DD4	A/S	34
8	DD5	CIK	33
9	CHB	INV	32
10	ΦB	INT/EXT	31
11	ΦA	GM0	30
12	MS	GM1	29
13	DA5	Y	28
14	DA6	GM2	27
15	DA7	DA4	26
16	DA8	DA3	25
17	V _{CC}	DA2	24
18	DA9	DA1	23
19	DA10	DA0	22
20	DA11	DA12	21

FIGURE 1 — BLOCK DIAGRAM OF USE OF THE VDG IN A TV GAME



Mnemonic	Pin Numbers	Function
VCC	17	+5V
VSS	1	Ground
CLK	33	Color burst clock 3.579545 MHz (input)
DA0-DA12	22, 23, 24, 25, 26 13, 14, 15, 16, 18, 19, 20, 21	Address lines to display memory, high impedance during memory select ($\overline{MS}$)
DD0-DD5	3, 4, 5, 6, 7, 8	Data from display memory RAM or ROM
DD6, DD7	2, 40	Data from display memory in graphic mode; data also in alpha external mode; color data in alpha semigraphic 4 or 6
$\phi A, \phi B, Y$	11, 10, 28	Chrominance and luminance analog (R-Y, B-Y, Y) output to RF modulator (MC1372)
CHB	9	Chroma bias; reference ϕA and ϕB levels
$\overline{RP}$	36	Row preset — Output to provide timing for external character generator.
$\overline{HS}$	38	Horizontal Sync — Output to provide timing for external character generator.
INV	32	Inverts video in all alpha modes
$\overline{INT}/EXT$	31	Switches to external ROM in alpha mode and between SEMIG-4 and SEMIG-6 in semigraphics
$\overline{A}/S$	34	Alpha/Semigraphics; selects between alpha and semigraphics in alpha mode
$\overline{MS}$	12	Memory select forces VDG address buffers to high-impedance state
$\overline{A}/G$	35	Switches between alpha and graphic modes
FS	37	Field Synchronization goes low at bottom of active display area.
CSS	39	Color set select; selects between two alpha display colors or between two color sets in semigraphics 6 and full graphics
GM0-GM2	30, 29, 27	Graphic mode select; select one of eight graphic modes.



ELECTRICAL SPECIFICATIONS

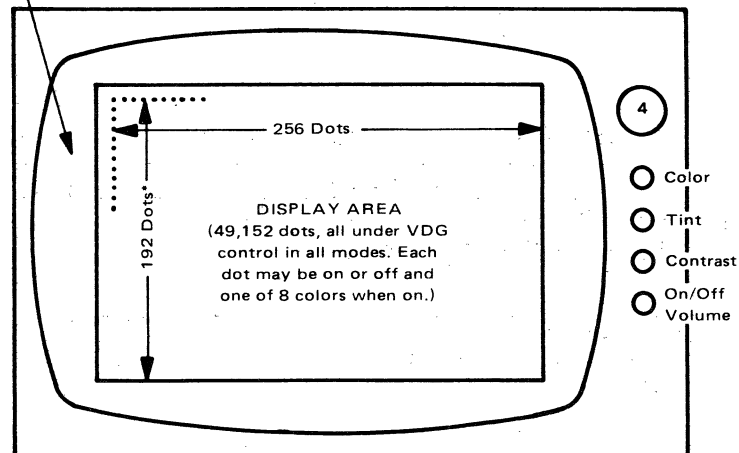
ABSOLUTE MAXIMUM RATINGS

Rating	Value
Supply Voltage (V_{CC})	-0.3 to +7.0V
Input Voltage any Pin	-0.3 to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Power Dissipation	TBD

FORMAT OF THE TELEVISION SCREEN

BORDER

(Black in all Alpha/Semigraphic Modes. Green or buff (off white) in all Graphic Modes. Controlled by the VDG.)



* One on each non-interlaced line.

DC (STATIC) CHARACTERISTICS — ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ.	Max.	Unit
Input High Voltage Clk Other Inputs	V_{IH}	$V_{SS} + 2.4$ $V_{SS} + 2.0$	— —	V_{CC} V_{CC}	Vdc
Input Low Voltage Clk Other Inputs	V_{IL}	$V_{SS} - 0.3$ $V_{SS} - 0.3$	— —	$V_{SS} + 0.4$ $V_{SS} + 0.8$	Vdc
Input Leakage Current CLK, GM0-GM2, INV, INT/EXT, MS, V_{SS} , DD0-DD7, A/S, A/G	I_{in}	—	—	2.5	μA_{dc}
Three-State (Off State) Input Current DA0-DA12	I_{LO}	—	—	10	μA_{dc}
Output High Voltage ($C_{Load} = 30 \text{ pF}$, $I_{Load} = -100 \mu\text{A}$) RP, HS, FS	V_{OH}	2.4	—	—	Vdc
Output High Voltage ($C_{Load} = 55 \text{ pF}$, $I_{Load} = -100 \mu\text{A}$) DA0-DA12	V_{OH}	2.4	—	—	Vdc
Output Load Voltage ($C_{Load} = 30 \text{ pF}$, $I_{Load} = 1.6 \text{ mA}$) RP, HS, FS	V_{OL}	—	—	$V_{SS} + 0.4$	Vdc
Output Low Voltage ($C_{Load} = 55 \text{ pF}$, $I_{Load} = 1.6 \text{ mA}$) DA0-DA12	V_{OL}	—	—	$V_{SS} + 0.4$	Vdc
Output High Current (Sourcing) ($V_{OH} = 2.4 \text{ V}$) All Outputs (except ϕA , ϕB , Y, & CHB)	I_{OH}	-100	—	—	μA_{dc}
Output Low Current (Sinking) ($V_{OL} = 0.4 \text{ Vdc}$) All Outputs (except ϕA , ϕB , Y, & CHB)	I_{OL}	1.6	—	—	mA_{dc}
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$) All Inputs	C_{in}	—	—	7.5	pF
Chroma Bias Voltage ($C_{Load} = 20 \text{ pF}$, R Load = 200 k ohm, $V_{CC} = 4.75 - 5.25 \text{ V}$)	V_R	—	$0.3 V_{CC}$	—	Vdc



DC (STATIC) CHARACTERISTICS — ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ.	Max.	Unit
Chroma ϕA Voltage ($C_{Load} = 20 \text{ pF}$, $R_{Load} = 200 \text{ k ohm}$)	$V_{C\phi A}$ V_{HI} V_O V_{LO}	— — — —	$V_R + 0.1 V_{CC}$ V_R $V_R - 0.1 V_{CC}$	— — —	Vdc
Chroma ϕB Voltage ($C_{Load} = 20 \text{ pF}$, $R_{Load} = 200 \text{ k ohm}$) V_O V_{burst} V_{LO}	$V_{C\phi B}$	— — — —	$V_R + 0.1 V_{CC}$ V_R $V_R - 0.05 V_{CC}$ $V_R - 0.1 V_{CC}$	— — — —	Vdc
Luminance Y Voltage ($C_{Load} = 20 \text{ pF}$, $R_{Load} = 200 \text{ k ohm}$)	V_Y V_S V_{BLANK} V_{BLACK}	— — — —	$0.2 V_{CC}$ $0.75 V_S$ $0.7 V_S$	— — —	Vdc
Voltage White Low (Voltage White Medium) (Voltage White High)	V_{WL} V_{WM} V_{WH}	— — —	$0.62 V_S$ $0.5 V_S$ $0.38 V_S$	— — —	Vdc

AC (Dynamic) CHARACTERISTICS — $V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C

Characteristic	Symbol	Min	Typ.	Max.	Unit
Clk Frequency	f	3.579535	3.579545	3.579555	MHz
Clk Duty Cycle	Clk _{dc}	45%	50%	55%	
Chroma Phase Delay (measured with respect to "Y" output)					ns
ϕA	t_{YA}	—	200	—	
ϕB	t_{YB}	—	200	—	
Luminance Rise Time	t_{ry}	—	60	—	ns
Luminance Fall Time	t_{fy}	—	50	—	
Chroma Rise and Fall Times (ϕA Rise Time) (ϕA Fall Time) (ϕB Rise Time) (ϕB Fall Time)	$t_{rC\phi A}$ $t_{fC\phi A}$ $t_{rC\phi B}$ $t_{fC\phi B}$	— — — —	60 60 60 60	— — — —	ns
Field Sync. (FS) (Pulse Width)	t_{WFS}	—	2.03	—	ms
Row Present (RP) (Pulse Width) (Delay From HS)	t_{WRP} t_{HSRP}	— —	0.98 0.98	— —	μs μs
Horizontal Sync (HS)	t_{WHS}	—	4.9	—	μs



FIGURE 2 – VIDEO AND CHROMINANCE RELATIONSHIPS OUTPUT WAVEFORM

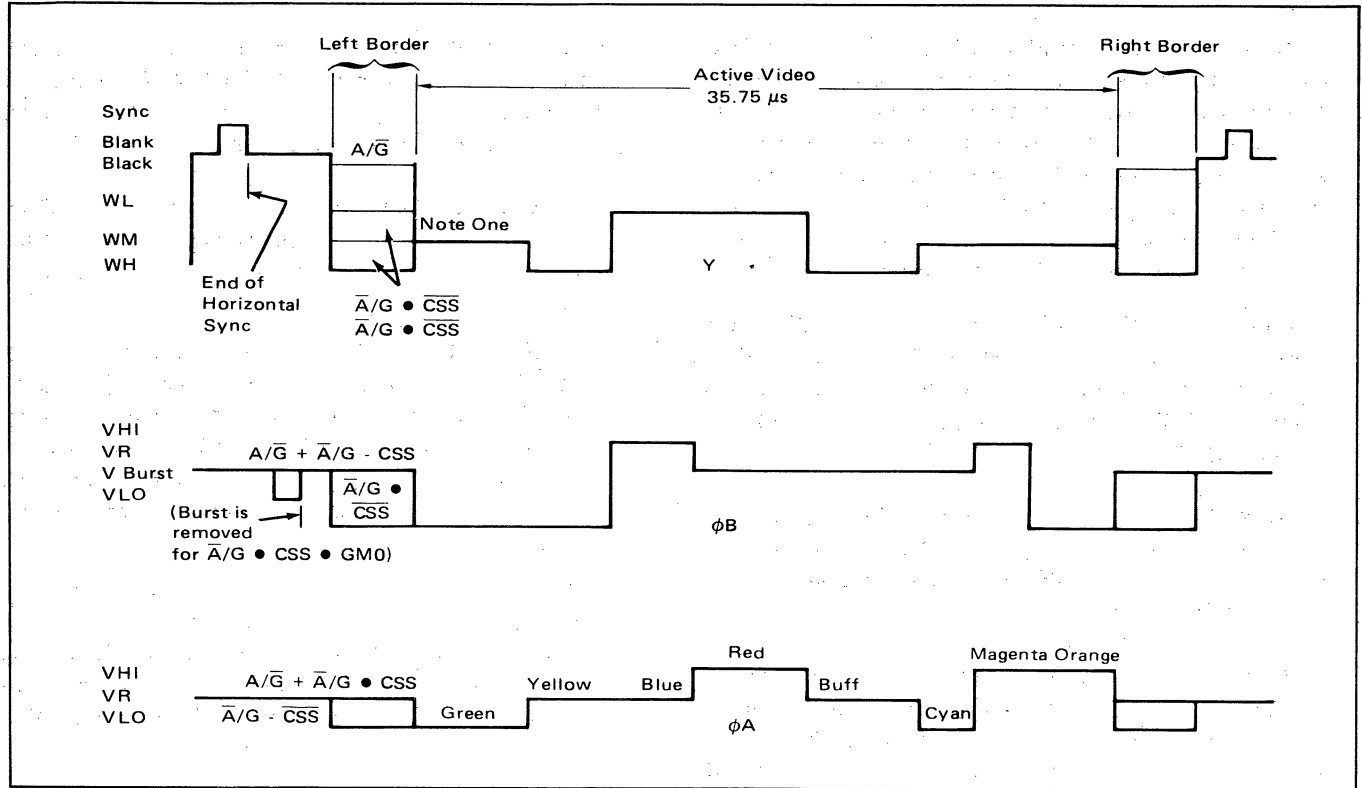
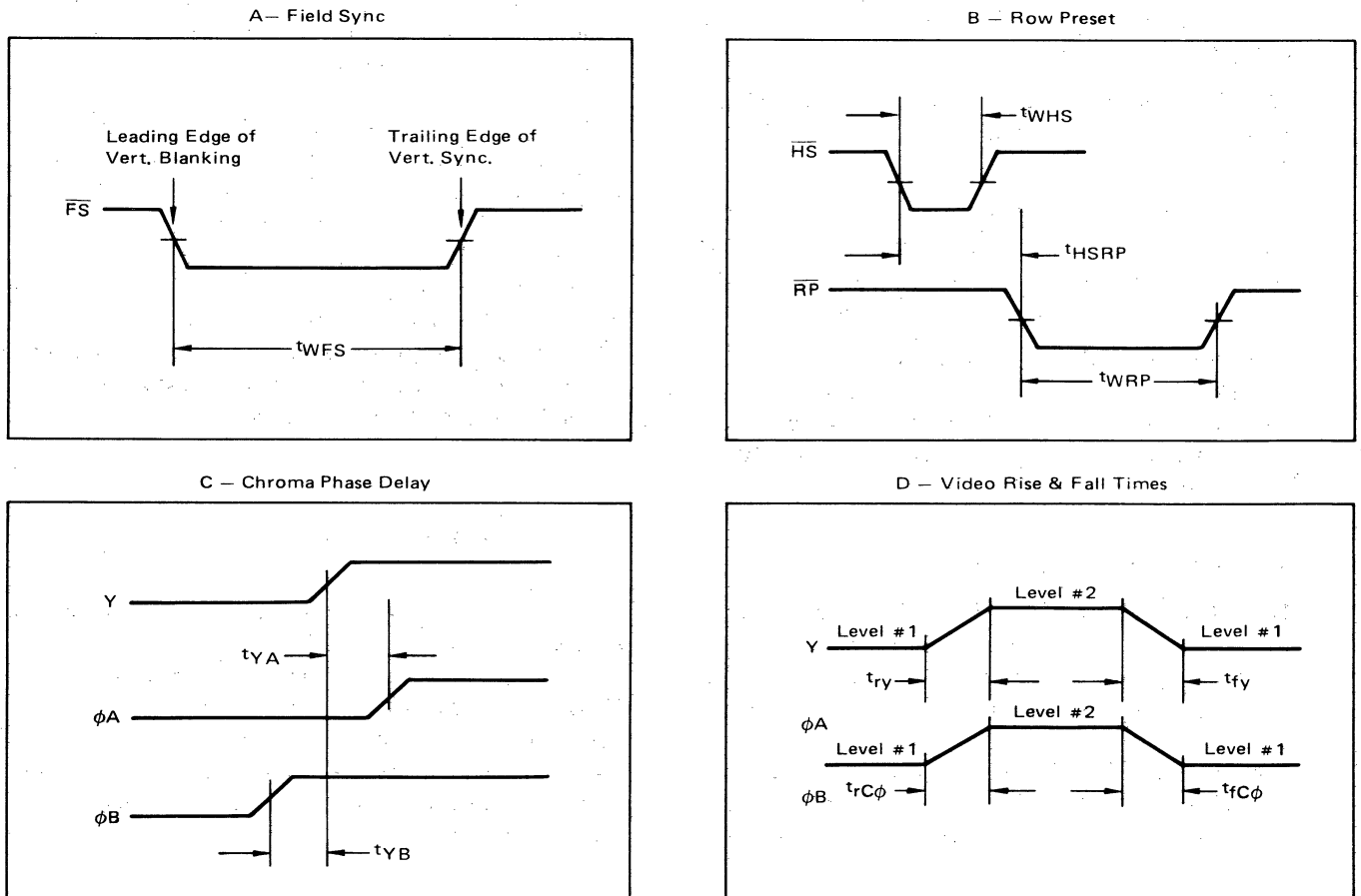


FIGURE 3 – TIMING DIAGRAMS



VDG SIGNAL DESCRIPTION

Address Output Lines (DA0-DA12) — Thirteen address lines are used by the VDG to scan the display memory. The starting address of the display memory is located at the upper left corner of the display screen. As the television sweeps from the left to right and top to bottom, the VDG increments the RAM display address. These lines are TTL compatible and may be forced into a high impedance state whenever the $\overline{MS}$ pin goes low.

Data Inputs (DD0-DD7) — Eight TTL compatible data lines are used to input data from RAM to be processed by the VDG. The data is interpreted and transformed into luminance Y (Pin 28) and color outputs ϕA and ϕB (Pin 11 and Pin 10).

Power Inputs — V_{CC} requires +5 volts. V_{SS} requires zero volts and is normally ground. The tolerance and current requirements of the VDG are specified in the Electrical Characteristics.

Video Outputs (ϕA , ϕB , Y, CHB) — These four analog outputs are used to transfer luminance and color information to a standard NTSC color television receiver, either via the MC1372 RF modulator or directly into Y, ϕA , ϕB television video inputs.

LUMINANCE (Y) — This six level analog output contains composite sync., blanking and four levels of video luminance.

ϕA — This three level analog output is used in combination with ϕB and Y outputs to specify one of eight colors.

ϕB — This four level analog output is used in combination with ϕA and Y outputs to specify one of eight colors. Additionally, one analog level is used to specify the time of the color burst reference signal.

CHROMA BIAS (CHB) — This pin is an analog output and provides a D.C. reference corresponding to the quiescent value of ϕA and ϕB . CHB is used to guarantee good thermal tracking and minimize the variation between the parts.

Synchronizing Inputs ($\overline{MS}$, CLK)

Three-State Control — ($\overline{MS}$) is a TTL compatible input which, when low, forces the VDG address lines into a high impedance state. This may be done to allow other devices (such as an MPU) to address the display memory (RAM).

Clock (CLK) — The VDG clock input (CLK) requires a 3.579545 MHz (standard) TV crystal frequency square wave. The duty cycle of this clock must be between 45

and 55 percent since it controls the width of alternate dots on the television screen. The MC1372 RF modulator may be used to supply the 3.579545 MHz clock and has provisions for a duty cycle adjustment.

Synchronizing Outputs ($\overline{FS}$, $\overline{HS}$, $\overline{RP}$) — Three TTL compatible outputs provide circuits, exterior to the VDG, with timing references to the following internal VDG states:

FIELD SYNC — ($\overline{FS}$) — The high to low transition of the $\overline{FS}$ output coincides with the end of active display area. During this time interval an MPU may have total access to the display RAM without causing undesired flicker on the screen. The Low to High transition of $\overline{FS}$ coincides with the trailing edge of the vertical synchronization pulse.

HORIZONTAL SYNC — ($\overline{HS}$) — The $\overline{HS}$ pulse is in coincident with the horizontal synchronization pulse furnished to the television receiver by the VDG. The high to low transition of the $\overline{HS}$ output coincides with the leading edge of the horizontal synchronization pulse.

ROW PRESET — ($\overline{RP}$) — If desired, an external character generator ROM may be used with the VDG. However, an external four bit counter must be added to supply row selection. The counter is clocked by the $\overline{HS}$ signal and cleared by the $\overline{RP}$ signal.

Mode Control Lines (Input) ($\overline{A/G}$, $\overline{A/S}$, $\overline{INT/EXT}$, GM0, GM1, GM2, CSS, INV) — Eight TTL compatible inputs are used to control the operating mode of the VDG. $\overline{A/S}$, $\overline{INT/EXT}$, CSS and INV may be changed on a character by character basis. The CSS pin is used to select between two possible alphanumeric colors; when the VDG is in the alphanumeric mode and between two color sets when the VDG is in the semigraphics 6 and full Graphic mode. Table 1 illustrates the various modes that can be obtained using the mode control lines.

DISPLAY MODES

The VDG is capable of generating 12 distinct display modes (refer to Table 1). The color set selection and invert pins will allow variations on certain modes. The VDG will display two alphanumeric modes with two compatible semigraphic modes or display one of eight full graphic modes. A detailed description of the various modes of operation follows. A summary of major modes can be found in Table 2.



ALPHANUMERIC DISPLAY MODES — All alphanumeric modes occupy an 8 x 12 dot character matrix box and there are 32 x 16 character boxes per TV frame. Each horizontal dot (dot-clock) corresponds to one-half the period duration of the 3.58 MHz clock and each vertical dot is one scan line. One of two colors for the lighted dots may be selected by the color set select pin. An internal ROM will generate 64 ASCII display characters in a standard 5 x 7 box. Six bits of the eight-bit data word are used for the ASCII character generator and the two bits not used can be used to implement inverse video or color switching on a character by character basis. A 512 word display memory is required for this class of display.

The ALPHA SEMIGraphics -4 mode translates bits zero through three into a 4 x 6 dot element in the standard 8 x 12 dot box. Three data bits may be used to select one of eight colors for the entire character box. The extra bit is available to implement mode switching on the fly. A 512 word display memory is required. A density of 64 x 32 elements is available in the display area. The element area is four dot-clocks wide by six lines high.

The ALPHA SEMIGraphic -6 mode maps six 4 x 4 dot elements into the standard 8 x 12 dot alphanumeric box, a screen density of 64 x 48 elements is available. Six bits are used to generate this map and two data bits may be used to select one of four colors in the display box. The element area is four dot-clocks wide by four lines high.

FULL GRAPHIC MODE — There are eight full graphic modes available from the VDG. These modes require 1K to 6K bytes of memory. The eight full-graphic modes include an outside color border in one of two colors depending upon the color set select pin (CSS). The CSS pin selects one of two sets of four colors in the four color graphic modes.

The 64 x 64 Color Graphics Mode — The 64 x 64 color graphics mode generates a display matrix of 64 elements wide by 64 elements high. Each element may be one of four colors. A 1K x 8 display memory is required. Each pictel equals four dot-clocks by three scan lines.

The 128 x 64 Graphics Mode — The 128 x 64 graphics mode generates a matrix 128 elements wide by 64 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors, selected by using the color set select pin. A 1K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 64 Color Graphics Mode — The 128 x 64 color graphics mode generates a display matrix 128 elements wide by 64 elements high. Each element may be one of four colors. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 96 Graphics Mode — The 128 x 96 graphics mode generates a display matrix 128 elements wide by 96 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors selected by using the color select pin. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 96 Color Graphics Mode — The 128 x 96 color graphics mode generates a display 128 elements wide by 96 elements high. Each element may be one of four colors. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 192 Graphics Mode — The 128 x 192 graphics mode generates a display matrix 128 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON elements may be one of two colors selected with color set select pin. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by one scan line.

The 128 x 192 Color Graphics Mode — The 128 x 192 color graphics mode generates a display 128 elements wide by 192 elements high. Each element may be one of four colors. A 3K x 8 display memory is required. A detailed description of the VDG modes is given in Table 3. Each pictel equals two dot-clocks by one scan line.

The 256 x 192 Graphics Mode — The 256 x 192 graphics mode generates a display 256 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON element may be one of two colors selected with the color set select pin. A 6K x 8 display memory is required. Each pictel equals one dot-clock by one scan line.



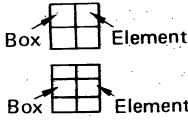
TABLE 1 — TABLE OF MODE CONTROL LINES (INPUTS)

$\overline{A}/G$	$\overline{A}/S$	$\overline{INT}/EXT$	INV	GM2	GM1	GM0	ALPHA/GRAPHIC MODE SELECT
0	0	0	0	X	X	X	Internal Alphanumerics
0	0	0	1	X	X	X	Internal Alphanumerics Inverted
0	0	1	0	X	X	X	External Alphanumerics
0	0	1	1	X	X	X	External Alphanumerics Inverted
0	1	0	X	X	X	X	Semigraphics - 4
0	1	1	X	X	X	X	Semigraphics - 6
1	X	X	X	0	0	0	64 x 64 Color Graphics
1	X	X	X	0	0	1	128 x 64 Graphics
1	X	X	X	0	1	0	128 x 64 Color Graphics
1	X	X	X	0	1	1	128 x 96 Graphics
1	X	X	X	1	0	0	128 x 96 Color Graphics
1	X	X	X	1	0	1	128 x 192 Graphics
1	X	X	X	1	1	0	128 x 192 Color Graphics
1	X	X	X	1	1	1	256 x 192 Graphics

TABLE 2 — SUMMARY OF MAJOR MODES

MAJOR MODE ONE

TABLE OF ALPHA MINOR MODES

Title	Memory	Colors	Display Elements
Alphanumeric (Internal)	512 x 8	2	
Alphanumeric (External)	512 x 8	2	
Alpha Semig-4	512 x 8	8	
Alpha Semig-6	512 x 8	4	

MAJOR MODE TWO

TABLE OF MINOR GRAPHICS MODES

Title	Memory	Colors	Comments
64 x 64 Color Graphic	1K x 8	4	Matrix 64 x 64 Elements
128 x 64 Graphics*	1K x 8	2	Matrix 128 elements wide by 64 elements high
128 x 64 Color Graphic	2K x 8	4	
128 x 96 Graphics*	1.5K x 8	2	Matrix 128 elements wide by 96 elements high
128 x 96 Color Graphic	3K x 8	4	
128 x 192 Graphics*	3K x 8	2	Matrix 128 elements wide by 192 elements high
128 x 192 Color Graphic	6K x 8	4	
256 x 192 Graphics*	6K x 8	2	Matrix 256 elements wide by 192 elements high

*Graphics mode turns on or off each element. The color may be one of two.

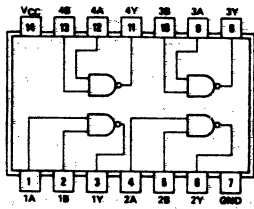


TABLE 3 – DETAILED DESCRIPTION OF VDG MODES

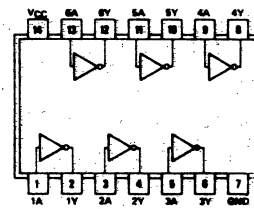
VDG PINS									COLOR			TV SCREEN		VDG DATA BUS	COMMENTS				
MS	A/G	A/S	INT/EXT	GM2	GM1	GM0	CSS	INV	Character Color	Background	Border	Display Mode	Detail						
1	0	0	0	X	X	X	0	0	Green	Black	Black	32 Characters across			The ALPHANUMERIC INTERNAL mode uses an internal character generator which contains the following five dot by seven dot characters: @ABCDEFGHIJ KLMNOPQRSTUVWXYZ[\] ! ~ \$ % & ' () * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ? . The six bit ASCII code leaves two bits free and these may be externally connected to the mode pins (A/G, A/S, INT/EXT, GM2, GM1, GM0, CSS or INV).				
							1	0	Orange	Black	Black	16 Characters down							
							1	1	Black	Orange	Black								
1	0	0	1	X	X	X	0	0	Green	Black	Black	32 Characters across			The ALPHANUMERIC EXTERNAL mode uses an external character generator as well as a row counter. Thus, custom character fonts are graphic symbol sets with up to 256 different eight dot x 12 dot "characters". may be displayed.				
							1	0	Orange	Black	Black	16 Characters down							
							1	1	Black	Orange	Black								
1	0	1	0	X	X	X	X	X	Lx	C2	C1	C0	Color	Black	64 Display elements across			The SEMIGRAPHICS FOUR mode uses an internal "course graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by three bits.	
									0	X	X	X	Black						32 Display elements down
									1	0	0	0	Green						
									1	0	0	1	Yellow						
									1	0	1	0	Blue						
									1	0	1	1	Red						
									1	1	0	0	Buff						
									1	1	0	1	Cyan						
									1	1	1	0	Magenta						
									1	1	1	1	Orange						
1	0	1	1	X	X	X	0	X	Lx	C1	C0	Color	Black	64 Display elements across			The SEMIGRAPHIC SIX mode is similar to the SEMIGRAPHIC FOUR mode with the following differences: The eight dot by twelve dot rectangle is divided into six equal parts. Color is determined by the two remaining bits.		
							1		0	0	0	Green						48 Display elements down	
							1		0	1	0	Yellow							
							1		1	1	0	Blue							
							1		1	1	1	Red							
							1		0	X	X	Black							
							1		0	0	0	Buff							
							1		0	1	1	Cyan							
							1		1	1	0	Magenta							
							1		1	1	1	Orange							
1	1	X	X	0	0	0	0	X	0	0	Color	Green	64 Display elements across			The GRAPHICS ONE C mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.			
							1		0	1	Blue						64 Display elements down		
1	1	X	X	0	0	1	0	X	0	0	Color	Green	128 Display elements across			The GRAPHICS ONE R mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element.			
							1		0	1	Black						64 Display elements down		
1	1	X	X	0	1	0	0	X	Same color as Graphics one C			Green	128 Display elements across			The GRAPHICS TWO C mode uses a maximum of 2048 bytes of display RAM in which one pair of bits specifies one picture element.			
							1										64 Display elements down		
1	1	X	X	0	1	1	0	X	Same color as Graphics one R			Green	128 Display elements across			The GRAPHICS TWO R mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.			
							1										96 Display elements down		
1	1	X	X	1	0	0	0	X	Same color as Graphics one C			Green	128 Display elements across			The GRAPHICS THREE C mode uses a maximum of 3072 bytes of display RAM in which one pair of bytes specifies one picture element.			
							1										96 Display elements down		
1	1	X	X	1	0	1	0	X	Same color as Graphics one R			Green	128 Display elements across			The GRAPHICS THREE R mode uses a maximum of 3072 bytes of display RAM in which one bit specifies one picture element.			
							1										192 Display elements down		
1	1	X	X	1	1	0	0	X	Same color as Graphics one C			Green	128 Display elements across			The GRAPHICS SIX C mode uses a maximum of 6144 bytes of display RAM in which one pair of bits specifies one picture element.			
							1										192 Display elements down		
1	1	X	X	1	1	1	0	X	Same color as Graphics one R			Green	256 Display elements across			The GRAPHICS SIX R mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element.			
							1										192 Display elements down		

APPENDIX H

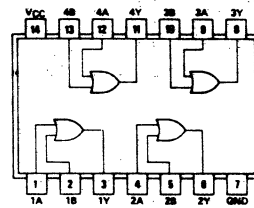
IC Pin Outs



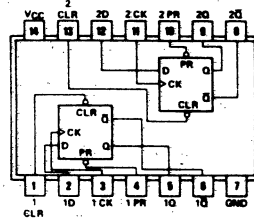
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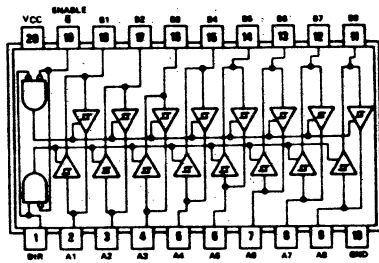
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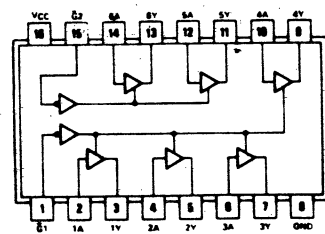
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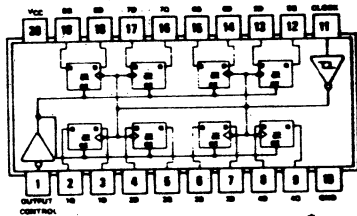
IC Pin Outs (Con't.)



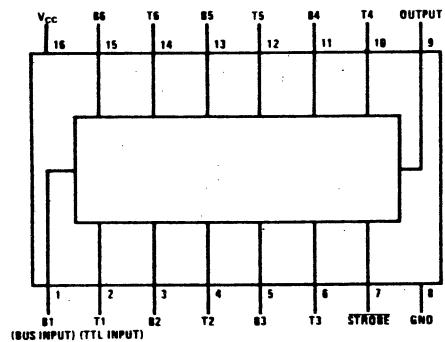
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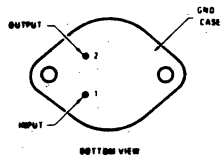
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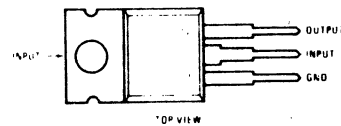
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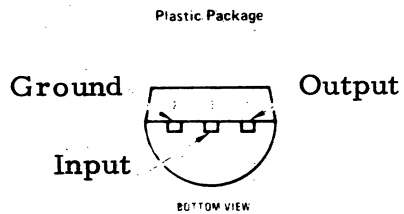
8131



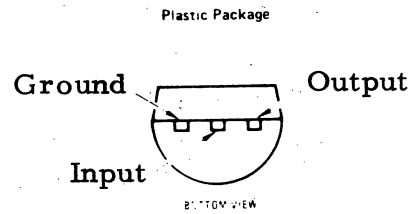
LM323-K



7812

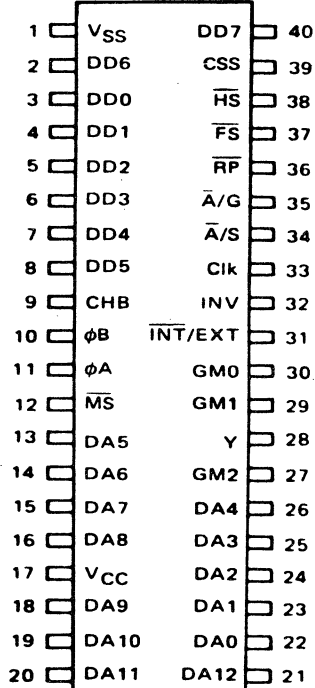


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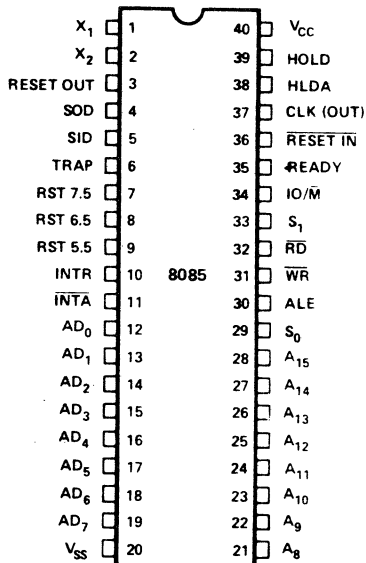


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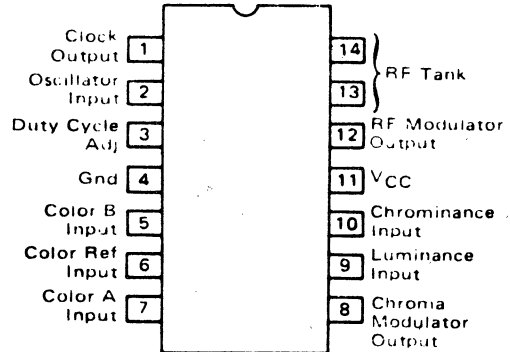
IC Pin Outs (Con't.)



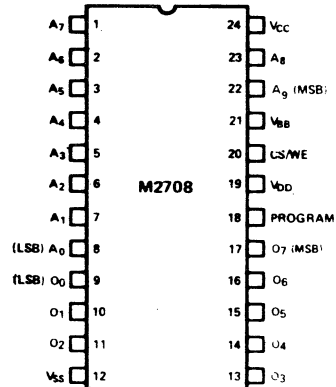
MC6847



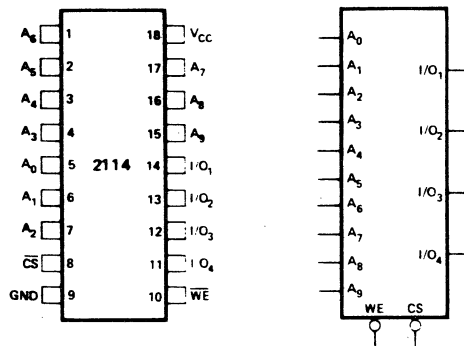
8085



MC1372



2708



2114

LIMITED WARRANTY

Biotech Electronics warrants for a period of 90 (ninety) days from the date of delivery to the customer, that the CGS-808A (Assembled and Tested) color graphics board described herein shall be free from defects in material and workmanship under normal use and service. This warranty shall be void if the board is altered or modified. During this period, if any defect should occur, the CGS-808 must be returned to Biotech Electronics for repair. Customer's sole and exclusive remedy in the event of a defect is expressly limited to the correction of the defect by adjustment or repair. Biotech Electronics will repair out-of-warranty product upon request from customer. Product may be returned to the factory upon receipt of a Return Authorization Number from the factory only. A service charge of \$25.00 will be assessed; plus the cost of any defective components (charges for the cost of defective components subject to customer approval).

Biotech Electronics warrants for a period of 60 (sixty) days from the date of delivery to the customer, that the CGS-808B (Bare "kit") color graphics printed circuit board described herein shall be free from defects in material and workmanship. No warranty will be extended to the MOS devices supplied with the CGS-808B (Bare "kit") — MC6847, MC1372, 8085, 2708 — due to the static sensitive nature of these devices. Biotech Electronics is not responsible for damage caused by the use of corrosive solder, defective tools, incorrect assembly, misuse, fire, or by unauthorized modifications to or uses of the CGS-808 for purposes other than as advertised. If the customer wishes to returned his/her CGS-808B (Bare "kit") for refund, he/she may do so before soldering any components onto the printed circuit board. The customer will be charged a 10% re-stocking charge. Biotech Electronics will repair the CGS-808B (Bare "kit") upon request from customer. Product may be returned to the factory upon receipt of a Return Authorization Number from the factory only. If the problem is a result of an etch error in the printed circuit board, the product will be repaired at no charge to the customer. If the problem is a result of faulty workmanship by the customer, a service charge of \$25.00 will be assessed; plus the cost of any defective components (charges for the cost of defective components subject to customer approval).

All Biotech Electronics computer programs are distributed on an "as is" basis without warranty.

This warranty covers only Biotech Electronics' products and is not extended to allied equipment or components used in conjunction with the CGS-808. Biotech Electronics is not responsible for incidental or consequential damages. Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply. This warranty gives specific legal rights, and the customer may also have other rights which vary from state to state.

APPENDIX K

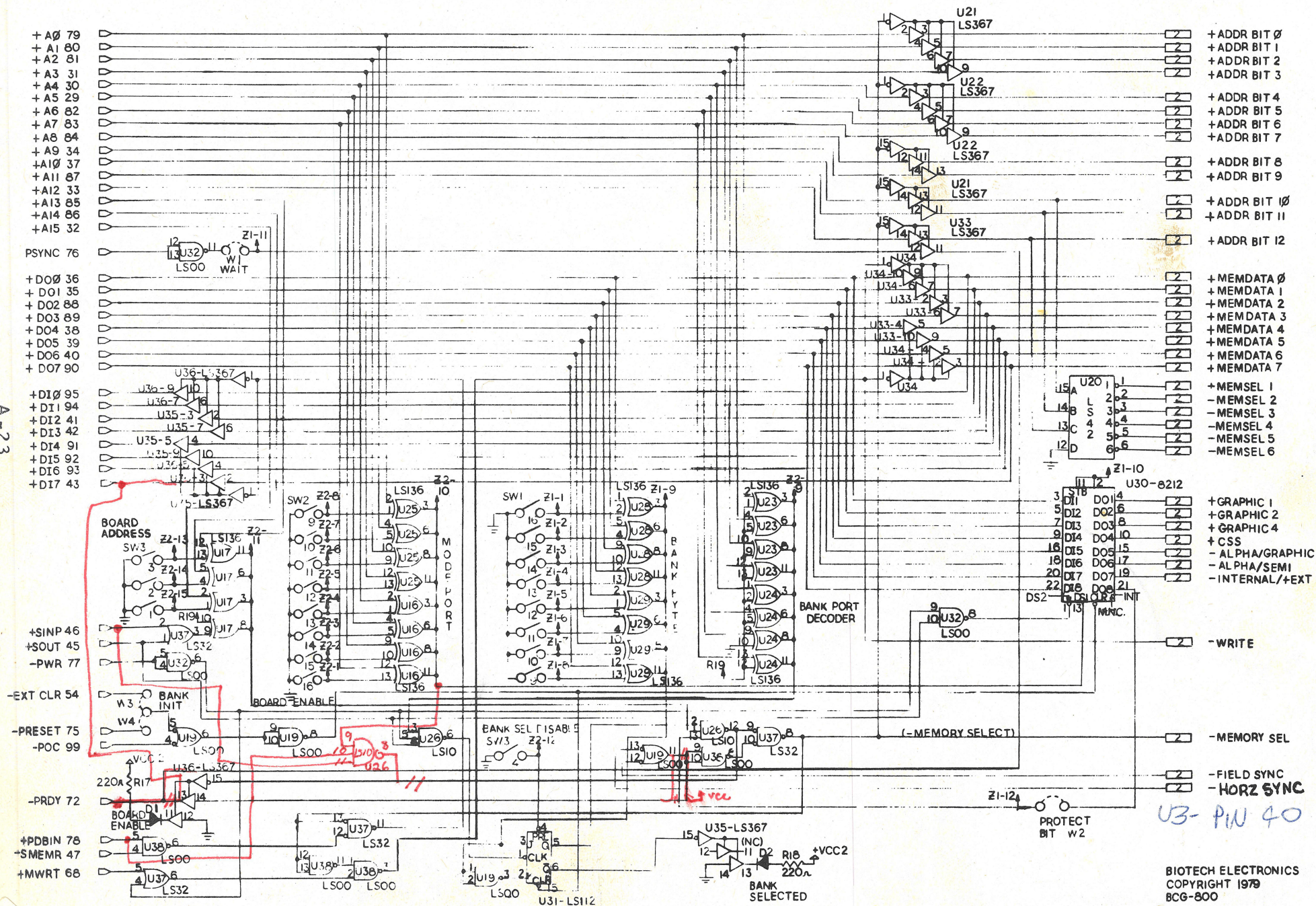
Resistor Color Code

Color	Significant Figure	Decimal Multiplier	Tolerance (%)
Black	0	1.00	
Brown	1	10.00	
Red	2	100.00	
Orange	3	1,000.00	
Yellow	4	10,000.00	
Green	5	100,000.00	
Blue	6	1,000,000.00	
Violet	7	10,000,000.00	
Gray	8	100,000,000.00	
White	9	1,000,000,000.00	
Gold	---	0.10	5
Silver	---	0.01	10
No Color	---	---	20

2530

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BCG-800

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